Curriculum Vitae – Daniele Ielmini

Present Position

Full Professor
Dipartimento di Elettronica, Informazione e Bioingegneria
Politecnico di Milano
Piazza L. da Vinci 32
20133 Milano – Italy

http://home.deib.polimi.it/ielmini/

Previous positions

2010 – 2016	Associate Professor, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano
2010	Visiting Professor, University of Illinois at Urbana-Champaign (UIUC)
2002 – 2010	Assistant Professor, Dipartimento di Elettronica e Informazione, Politecnico di Milano
2006	Visiting Professor, Intel Corporation and Center for Integrated Systems (CIS) – Stanford University
2000 – 2002	Research Assistant, Dipartimento di Elettronica e Informazione, Politecnico di Milano

Education

1997 – 2000	Ph.D., Nuclear Engineering, Politecnico di Milano
1989 – 1995	Laurea, Nuclear Engineering, Politecnico di Milano

Awards and Recognition

2019	Fellow, IEEE
2015	Highly Cited Researcher, Thomson Reuters
2014	ERC Consolidator Grant
2013	Intel Outstanding Researcher Award for Devices
2009	Senior Member, IEEE

Best Paper Awards

2019	Technology Best Student Paper Award of the 2019 VLSI Symposia for the paper “Energy-Efficient Continual Learning in Hybrid Supervised-Unsupervised Neural Networks with PCM Synapses,” by S. Bianchi, I. Muñoz-Martin, G. Pedretti, O. Melnic, S. Ambrogio and D. Ielmini, presented by S. Bianchi at the 2019 Symposium on VLSI Technology.
2019	WiCAS (Women in Circuits And Systems) 2019 Best Paper award for the paper "A Volatile RRAM Synapse for Neuromorphic Computing" by E. Covi, Y.-H. Lin, W. Wang, T. Stecconi, A. Bricalli, E. Ambrosi, G. Pedretti, T.-Y. Tseng, and D. Ielmini, presented by E. Covi et the IEEE International Conference on Electronics Circuits and Systems (ICECS).
2015	IEEE EDS Paul Rappaport Award for the paper “Noise-Induced Resistance Broadening in Resistive Switching Memory—Part I: Intrinsic Cell Behavior and Part II: Array Statistics,” by S. Ambrogio, S. Balatti, V. McCaffrey, D. C. Wang, and D. Ielmini, as the best paper in the IEEE Trans. Electron Devices over 630 papers that were published in 2015.
2014	Best Poster Award for the paper “Voltage-Dependent Random Telegraph Noise (RTN) in HfO_x Resistive RAM,” by S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, presented by S. Balatti at the International Reliability Physics Symposium (IRPS) 2014
2013	Best Paper Award for the paper “Resistive Switching in Metal Oxides: From Physical Modeling to Device Scaling,” by D. Ielmini, S. Balatti, and S. Ambrogio, presented by D. Ielmini at 224th ECS, Oct 27-Nov 1, 2013.
2011	Best Student Paper Award for the paper “Filament diffusion model for simulating reset and retention processes in RRAM,” by S. Larentis, C. Cagli, F. Nardi and D. Ielmini, presented by S. Larentis at the Insulating Films on Semiconductors (INFOS) 2011
2007	Impressive Award for Best Presentation at the European Phase Change and Ovonic Science Symposium, E/PCOS 2007

Conference Organizations

2017 – 2018	International Electron Device Meeting (IEDM), Subcommittee Member for Memory Technology
2018 – 2019	NANOARCH, Member of the Program Committee
2017	Design, Automation, and Test in Europe (DATE), Member of the Technical Committee
2017	ISCAS, organized the Special Session ‘Computing with memory devices’

2016 – 2021	ISCAS, Member of the NanoGiga Technical Committee
2015 – 2019	European Phase Change and Ovonic Science Symposium (E/PCOS), Member of the Program Committee
2015	European Material Research Symposium (EMRS), Member of the Scientific Committee
2014	CAS-FEST 2014, Special Session Organizer
2014 – 2018	CIMTEC, Forum of Novel Materials, Member of the Technical Committee
2013	PACRIM10, Member and Contact of the Technical Committee
2013 – 2019	Chinese Semiconductor Technology International Conference (CSTIC), Member of the Technical Committee
2012	NonVolatile Memory Technology Symposium (NVMTS), Session Chair
2012	European Material Research Symposium (EMRS), Member of the Scientific Committee
2011 – 2017	Insulating Films on Semiconductors (INFOS), Member of the Technical Committee
2008 – 2010	Semiconductor Interface Specialist Conference (SISC), Member of the Technical Committee
2008 – 2009	International Electron Device Meeting (IEDM), Subcommittee Member for Memory Technology
2007	International Reliability Physics Symposium (IRPS), Workshop organizer and moderator for Non volatile memory
2006 – 2008	International Reliability Physics Symposium (IRPS), Subcommittee Member for Dielectrics and Memory

Instructor

2021	Tutorial on “In-memory computing with emerging memory devices: status and challenges,” International Integrated Reliability Workshop (IIRW), Lake Tahoe, Oct. 4-29, 2021.
2021	Tutorial on “Analogue linear algebra accelerators,” International Memory Workshop (IMW), Dresden, May 16-19, 2021.
2020	Tutorial on “Resistive switching memory for in-memory computing applications,” European Solid-State Device Research Conference (ESSDERC), Sept. 14-18, 2020.
2019	Tutorial on “Emerging nonvolatile memory technologies,” IEEE Electron Device Technology and Manufacturing (EDTM), Singapore, Mar. 12-15, 2019.
2018	Tutorial on “Embedded memory technologies,” IEEE International Conference on IC Design and Technology (ICICDT), Otranto, Italy, June 4-6, 2018.
2017	Tutorial on “Resistive memory: switching mechanisms, models, and applications in computing,” 2017 SIE Meeting, Palermo, Italy, June 19-23, 2017.
2017	Tutorial on “Memristive devices, circuits, systems and applications,” 2017 IEEE-ISCAS, Baltimore, MD, USA, May 28-31, 2017.
2017	Tutorial on “Physics of emerging devices,” 2017 International Memory Workshop (IEEE-IMW, 2017), Monterey, CA, USA, May 14-17, 2017.
2017	Lecture on “High density ReRAM and PCRAM,” 2017 1st Electron Devices Technology and Manufacturing Conference (IEEE-EDTM, 2017)
2016	Tutorial on Memristive devices and neuromorphic networks, Material Research Society Fall Meeting (MRS 2016)
2016	Tutorial on Memristive Theory and Modeling, Second Training Course on Memristors - Devices, Models, Circuits, Systems and Applications (MemoCIS), Alghero, May 7-9 (2016)
2015	Lecture on “Emerging memory technologies: ReRAM and PCM”, in 2015 IEDM short course on “Memory Technologies for Future Systems”, Washington DC, USA, Dec. 7-9 (2015)
2015	Tutorial on Memristive Switching Mechanisms, First Training Course on Memristors - Devices, Models, Circuits, Systems and Applications (MemoCIS), Alghero, May 9-12 (2015)
2013	Tutorial on Resistive switching memory mechanisms, International Memory Workshop (IEEE-IMW 2013)
2012	Tutorial on Resistive switching memory modeling, Material Research Society Spring Meeting (MRS 2012)
2011	Tutorial on Phase change memory modeling, Material Research Society Spring Meeting (MRS 2011)
2011	Tutorial on Resistance switching and memristive computing, Nano Giga Challenges (NGC 2011)
2010	Tutorial on Phase change memories, Material Research Society Spring Meeting (MRS 2010)
2010	Tutorial on Memory Reliability, European Symposium on Reliability and Failure (ESREF 2010)
2008	Tutorial on Non-Volatile Memories, International Reliability Physics Symposium (IRPS 2008)
2007	Tutorial on Memory Reliability, International Reliability Physics Symposium (IRPS 2007)
2005	Tutorial on Memory Reliability, International Reliability Physics Symposium (IRPS 2005)

Teaching

2002 – 2021	Solid State Electronics, Undergraduate Student Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/ess.htm)
2006 – 2015	Nonvolatile memories, PhD Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/nvm.htm)
2015 – 2021	Optoelectronics, Undergraduate Student Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/oe.htm)
2015 – 2019	New materials and devices for post-Si computing, PhD Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/psc.htm)
2000 – 2008	Fundamental of Electronics, Undergraduate Student Course, EE, Politecnico di Milano
2008	Nonvolatile Resistive Memories, Graduate Students Course, Master in Technologies for Micro-Nano Electronics, Università degli Studi di Roma ‘La Sapienza’

Editorial activities

2021	Semiconductor Science and Technology (IOP), Guest Editor for a Special Issue on 'Neuromorphic Devices and Applications', Guest Editors: D. Ielmini, T.-H. Hou, J. Kim, M. Liu, M. Suri
2017	J. Electroceramics (Springer), Guest Editor for a Special Issue on 'Resistive Switching: Oxide Materials, Mechanisms, Devices and Operations', guest editors: D. Ielmini, J. Rupp and I. Valov
2017 – 2021	Semiconductor Science and Technology (IOP), Associate Editor
2015 – 2021	IEEE Trans. Nanotechnology, Associate Editor

Journal Reviewer

Science, Nature, Nature Nanotechnology, Nature Communications, Nature Materials, Nature Electronics, Science Advances, Scientific Reports, Advanced Materials, Advanced Functional Materials, Nano Letters, ACS Nano, Nanoscale, IEEE Transactions on Electron Devices, IEEE Electron Device Letters, Nanotechnology, and others.

Professional Memberships

Institute of Electrical and Electronics Engineers (IEEE, Fellow)

General Research Interests

Research interests are focused on CMOS and post-CMOS devices and circuits, particularly regarding the characterization and modeling of memory devices and their scaling challenges. My research activity has been devoted to the following topics:

- CMOS front-end reliability (dielectric trapping and leakage effects, hot carrier effects, NBTI)
- Modeling and characterization of CMOS-based non-volatile memories (Flash, nanocrystal, charge-trap memories)
- Modeling and characterization of emerging nonvolatile memories (phase change memory – PCM, resistive switching memory – RRAM, conductive bridge memory – CBRAM, spin-torque transfer magnetic memory – STTRAM)
- In-memory computing and neuromorphic computing

Ph.D./Postdoc Student Supervisor

Christian Monzio Compagnoni (Ph.D., 2005, now Associate Professor at Politecnico di Milano, Italy)
Deepak Sharma (Post doc, 2006 – 2008, now Professor at SCRIET, Meerut, India)
Davide Mantegazza (MS 2004, Ph.D. 2008, now with Intel)
Ugo Russo (MS 2005, Ph.D. 2009, now with Micron)
Simone Lavizzari (MS 2006, Ph.D. 2010, now with Prophesee)
Carlo Cagli (MS 2007, Ph.D. 2011, now with CEA-LETI)
Davide Fugazza (Ph.D. 2011, now with Intel)
Mattia Boniardi (Ph.D. 2011, now with Technoprobe)
Federico Nardi (MS 2008, Ph.D. 2012, now with Applied Materials)
Maurizio Rizzi (MS 2011, Ph.D. 2014, now with Micron)
Seol Choi (Post doc, 2011-2012, now with Samsung)
Nicola Ciocchini (MS 2011, Ph.D. 2015, now with Micron)
Simone Balatti (MS 2011, Ph.D. 2015, now with Applied Materials)
Stefano Ambrogio (MS 2012, Ph.D. 2016, now with IBM)
ZhongQiang Wang (Post doc, 2014-2016, now Full Professor at Northeast Normal University, Changchun, China)
Mario Laudato (MS 2014, Ph.D. 2018, now with Intermolecular)
Valerio Milo (MS 2015, Ph.D. 2019, now with Applied Materials)
Alessandro Bricalli (MS 2015, Ph.D. 2019, now with Weebit Nano)
Elia Ambrosi (MS 2016, Ph.D. 2020, now with TSMC)
Roberto Carboni (MS 2016, Ph.D. 2020, now with Intel)
Giacomo Pedretti (MS 2016, Ph.D. 2020, now with HP)
Nicola Polino (MS 2016, Ph.D. expected in 2022)
Zhong Sun (Post doc, 2017-2019, now Assistant Professor at Peking University)
Wang Wei (Post doc, 2017-2020, now postdoc at Technion, Israel)
Stefano Bianchi (MS 2017, Ph.D. 2021, now with Infineon)
Irene Munoz (Ph.D. 2021, now with Infineon)
Octavian Melnic (MS 2017, Ph.D. expected in 2022)
Erika Covi (Post doc, 2018-2020, now with NamLab)
Shahin Hashemkhani (MS 2019, Ph.D. expected in 2023)
Saverio Ricci (Ph.D. expected in 2023)
Matteo Farronato (MS 2019, Ph.D. expected in 2023)
Piergiulio Mannocci (MS 2020, Ph.D. expected in 2024)
Matteo Baldo (MS 2020, Ph.D. expected in 2024)
Nicola Lepri (MS 2020, Ph.D. expected in 2024)
Alessandro Milozzi (MS 2020, Ph.D. expected in 2024)
Lorenzo Cattaneo (MS 2021, Ph.D. expected in 2024)
Artem Glukhov (MS 2021, Ph.D. expected in 2024)

List of Publications

Books

[1] Resistive switching – from fundamental redox-processes to device applications (Wiley-VCH, 2016), D. Ielmini and R. Waser Eds. (2016). ISBN 978-3-527-33417-9
[2] Resistive Switching: Oxide Materials, Mechanisms, Devices and Operations (Springer, 2022), J. Rupp, D. Ielmini and I. Valov Eds. (2022). ISBN 978-3-030-42423-7 DOI: 10.1007/978-3-030-42424-4

Book Chapters

[3] D. Ielmini, "Phase change memory device modeling," in Phase Change Materials – Science and Applications, Springer, S. Raoux and M. Wuttig Eds., 299-330 (2009). ISBN 978-0-387-84873-0.
[4] C. Monzio Compagnoni, R. Gusmeroli, A. S. Spinelli, D. Ielmini, A. L. Lacaita and A. Visconti, "Present status and scaling challenges for the NOR Flash memory technology," in Solid State Electronics Research Advances, Nova Science Publishers, Inc., New York, Sergo Kobadze ed., 101-134 (2009). ISBN 978-1-60021-851-4.
[5] C. Cagli and D. Ielmini, "Resistive-Switching Memory Devices Based on Metal Oxides: Modeling of Unipolar Switching, Reliability, and Scaling," in Nonvolatile Memories: Materials, Devices and Applications, edited by Tseung-Yuen Tseng and Simon M. Sze, Volume 2, 225-248 (American Scientific Publishers, 2012). ISBN 1-58883-251-1
[6] D. Ielmini, "Phase Change Memory Physics-Based Modeling: Electrical Characteristics, Scaling, and Reliability," in Nonvolatile Memories: Materials, Devices and Applications, edited by Tseung-Yuen Tseng and Simon M. Sze, Volume 2, 83-109 (American Scientific Publishers, 2012). ISBN 1-58883-251-1
[7] D. Ielmini, "Resistive switching models by ion migration in metal oxides," in Nanoscale Applications for Information and Energy Systems, Series: Nanostructure Science and Technology, Anatoli Korkin and David J. Lockwood (Eds.), XII, 346, 169-202 (Springer, 2013). ISBN 978-1-4614-5015-3. DOI: 10.1007/978-1-4614-5016-0_6
[8] D. Ielmini, "Resistive switching memories," in Wiley Encyclopedia Electrical and Electronic Engineering (EEEE), J. Webster (ed.), 1-32 (2014 John Wiley & Sons, Inc.). DOI: 10.1002/047134608X.W8222. ISBN: 0-471-13946-7.
[9] R. Waser, D. Ielmini, H. Akinaga, H. Shima, H.-S. Philip Wong, J. J. Yang, and S. Yu, "Introduction to Nanoionic Elements for Information Technology," in Resistive switching – from fundamental redox-processes to device applications, (Wiley-VCH, 2016), D. Ielmini and R. Waser Eds. (2016). ISBN 978-3-527-33417-9
[10] D. Ielmini, and S. Menzel, "Universal Switching Behavior," in Resistive switching – from fundamental redox-processes to device applications, (Wiley-VCH, 2016), D. Ielmini and R. Waser Eds. (2016). ISBN 978-3-527-33417-9
[11] D. Ielmini, "Electrical Transport in crystalline and amorphous chalcogenide," in Phase Change Memory: Device Physics, Reliability and Applications, (Springer International Publishing AG 2018), A. Redaelli Ed. 11-39 (2018). ISBN: 978-3-319-69052-0, DOI: 10.1007/978-3-319-69053-7
[12] D. Ielmini and V. Milo, "Brain-inspired memristive neural networks for unsupervised learning," in Handbook of Memristor Networks, G. Sirakoulis and L. Chua eds. 495-525 (Springer, Cham, 2019). doi: 10.1007/978-3-319-76375-0_17
[13] D. Ielmini and S. Ambrogio, "Neuromorphic computing with resistive switching memory devices," in Advances in Non-volatile Memory and Storage Technology, 2nd Edition, B. Magyari-Kope and Y. Nishi eds. 603-631 (Elsevier, 2019). Doi: 10.1016/B978-0-08-102584-0.00017-6
[14] R. Carboni and D. Ielmini, "Applications of Resistive Switching Memory as Hardware Security Primitive," in: M. Suri (eds) Applications of Emerging Memory Technology. Springer Series in Advanced Microelectronics, vol 63, 93-131 (Springer, Singapore, 2020). Doi: 10.1007/978-981-13-8379-3_4
[15] V. Milo, T. Dalgaty, D. Ielmini, E. Vianello, "Synaptic realizations based on memristive devices," in Memristive devices for brain-inspired computing 427-477 (Elsevier, 2020). Doi: 10.1016/B978-0-08-102782-0.00017-4
[16] V. Milo, G. Malavena, C. Monzio Compagnoni and D. Ielmini, "Memristive/CMOS devices for neuromorphic applications," in Springer Handbook of Semiconductor Devices, edited by Massimo Rudan, Rossella Brunetti and Susanna Reggiani (Springer, 2021).
[17] D. Ielmini, "Drift Phenomena in Phase Change Memories," in A. Kolobov (eds) Reference of Amorphous Materials (World Scientific, 2021). Doi: 10.1142/11697-vol1
[18] G. Pedretti and D. Ielmini, "Computing with nonvolatile memories for artificial intelligence," in A. Redaelli and F. Pellizzer (eds) Semiconductor Memory and Systems (Elsevier, 2021).

Invited Papers in Journals and Conference Proceedings

[19] A. Pirovano, A. Redaelli, F. Pellizzer, F. Ottogalli, M. Tosi, D. Ielmini, A. L. Lacaita and R. Bez, "Reliability study of phase-change non-volatile memories," IEEE Trans. on Device and Material Reliability 4, 422-427 (2004).
[20] D. Ielmini, A. S. Spinelli and A. L. Lacaita, "Recent developments on Flash memory reliability," Proc. INFOS 2005, published on special issue of Microelectron. Eng. 80C, 321-328 (2005).
[21] C. Monzio Compagnoni, R. Gusmeroli, D. Ielmini, A. S. Spinelli, A. L. Lacaita, "Silicon nanocrystal memories: a status update," Journal of Nanoscience and Nanotechnology 7, 193-205 (2007).
[22] D. Ielmini and A. L. Lacaita, "Physical modeling of conduction and switching mechanisms in phase change memory cells," European Phase Change and Ovonics Science Symposium, E*PCOS (2007).
[23] A. L. Lacaita and D. Ielmini, "Status and challenges of phase change memory modeling," European Solid-State Device Research Conference, ESSDERC, 214-221 (2007).
[24] A. L. Lacaita and D. Ielmini, "Reliability issues and scaling projections for phase change non volatile memories," IEDM Tech. Dig.,157-160 (2007).

[25] A. L. Lacaita, U. Russo and D. Ielmini, “Recent advances on the modeling of phase change materials and devices,” Mater. Res. Soc. Symp. Proc. 1072-G06-05 (2008).
[26] D. Ielmini, “Modeling of switching phenomena in phase-change memory (PCM) devices,” Proc. European Phase-Change and Ovonic Symposium (E*PCOS), 99-108 (2008).
[27] D. Ielmini, “Reliability issues and modeling of Flash and post-Flash memory,” Insulating Films on Semiconductors – INFOS, Cambridge, UK (June 2009), also appearing in Microelectron. Eng. 86, 1870-1875 (2009).
[28] D. Ielmini, “Reliability and scaling challenges of phase-change memories from a physical-modeling perspective,” 4th International Symposium on Next-generation Non-volatile Memory Technology for Terabit Memory, 131-132 (2009).
[29] D. Ielmini, “Overview of modeling approaches for scaled non-volatile memories,” Proc. International Conference on Simulation of Semiconductor Processes and Devices, SISPAD, 9-16 (2009). ISBN 978-1-4244-3947-8.
[30] A. L. Lacaita and D. Ielmini, “Bridging carrier transport and amorphous dynamics in phase change materials,” Proceedings of the 2009 European Phase-Change and Ovonic Symposium (E*PCOS), 165-173 (2009).
[31] D. Ielmini, “Modeling of resistance switching and reliability in non-volatile PCM and RRAM,” Proc. International Symposium on Integrated Ferroelectrics and Functionalities, ISIF2 108 (2009).
[32] S. Raoux, W. Welnic and D. Ielmini, “Phase change materials and their application to non-volatile memories,” Chem. Rev. 110, 240-267 (2010).
[33] D. Ielmini, “Understanding phase change memory reliability and scaling by physical models of the amorphous chalcogenide phase,” Mater. Res. Soc. Symp. Proc. 1251-H05-01 (2010).
[34] D. Ielmini, “Scaling effects of programming and reliability in phase change memory,” ISIF 302-303 (2010).
[35] D. Ielmini, “Size-dependent switching and reliability of NiO RRAMs,” ECS Trans. 33, 3, 323-331 (2010).
[36] D. Ielmini, “Unified physical model of reliability mechanisms and scaling perspective of phase change memory,” Current Applied Phys. 11, e85-e91 (2011).
[37] D. Ielmini, “Universal set/reset characteristics of metal-oxide resistance switching memories,” ECS Trans. 35, 4, 581-596 (2011).
[38] D. Ielmini, D. Fugazza and M. Boniardi, “Energy landscape models for conduction and drift in PCM,” Mater. Res. Soc. Symp. Proc. Vol. 1338 (2011).
[39] D. Ielmini, R. Bruchhaus and R. Waser, “Thermochemical resistive switching: Materials, mechanisms and scaling projections,” Phase Transition 84, 7, 570–602 (2011). DOI:10.1080/01411594.2011.561478
[40] D. Ielmini and D. Fugazza, “Size-dependent random-telegraph noise in phase-change memory (PCM) devices,” EPCOS (2011).
[41] D. Ielmini and A. L. Lacaita, “Phase change materials in non-volatile storage,” Materials Today 14, 600-607 (2011).
[42] D. Ielmini and A. L. Lacaita, “Electrical properties and microscopic structure of amorphous chalcogenides,” Nonvolatile Memory Technology Symposium (2011).
[43] D. Ielmini, “Filamentary-switching model in RRAM for time, energy and scaling projections,” IEDM Tech. Dig. 409-412 (2011).
[44] D. Ielmini, “Phase change memory modeling: From chalcogenide physics to device scaling,” ECS Transactions – CSTIC 2012, Vol. 44, 1227-1234 (2012).
[45] S. Raoux, D. Ielmini, M. Wuttig and I. V. Karpov, “Phase change materials,” MRS Bull. 37, 118-123 (2012).
[46] D. Ielmini, S. Larentis, S. Balatti, F. Nardi and D. Gilmer, “Ion migration model for resistive switching in transition metal oxides,” Nanosession Kick-off Talk, Nature Conference, Technical Digest of Frontiers in Electronic Materials, J. Heber, D. Schlom, Y. Tokura, R. Waser and M. Wuttig, (Eds.), Wiley-VCH, 219-220 (2012). ISBN 978-3-527-41191-7
[47] D. Ielmini, “Switching models for bipolar RRAM devices,” Workshop on Dielectrics in Microelectronics (WoDiM), Dresden, Germany, June 2012.
[48] D. Ielmini, S. Balatti and S. Larentis, “A Physics-based Model of Resistive Switching in Metal Oxides,” International Conference on Solid State Devices and Materials (SSDM), Kyoto, Japan, 25-27 Sept. 2012.
[49] D. Ielmini, “Physical modeling of voltage-driven resistive switching in oxide RRAM,” IEEE International Integrated Reliability Workshop (IIRW) Final Report 9-15 (2012). DOI:10.1109/IIRW.2012.6468905
[50] D. Ielmini, “Modeling of ion-based resistive switching in metal oxides,” NVMTS, Singapore 31 Oct.-2 Nov. 2012.
[51] D. Ielmini, “Electron and ion transport models in metal oxide RRAM,” APS Spring Meeting (2013).
[52] D. Ielmini, “Resistive switching in high-k metal oxides: modeling and scaling,” Mater. Res. Soc. Symp. Proc. (2013).
[53] D. Ielmini, “Resistive switching nanodevices: Models, scaling and applications,” China NANO, Sept. 4-6, 2013.
[54] N. Ciocchini, M. Cassinerio and D. Ielmini, “Crystallization phenomena in phase change memories: non-Arrhenius kinetics, modeling and novel applications,” Proc. European Phase-Change and Ovonic Symposium (E*PCOS) (2013).
[55] A. Behnam, F. Xiong, K. L. Grosse, A. Cappelli, S. Hong, N. Wang, M.-H. Bae, Y. Dai, A.D. Liao, E.A. Carrion, D. Ielmini, E. Piccinini, C. Jacoboni, W. P. King, and E. Pop, “Sub-10 nm Scaling of Phase-Change Memory: Thermoelectric Physics, Carbon Nanotube and Graphene Electrodes,” Proc. European Phase-Change and Ovonic Symposium (E*PCOS) (2013).
[56] D. Ielmini, S. Ambrogio and S. Balatti, “Resistive switching in metal oxides: from physical modeling to device scaling,” in ECS Transactions 58, 165-173 (2013). DOI: 10.1149/05807.0165ecst
[57] S. Ambrogio, S. Balatti, A. Cubeta, D. Ielmini, “Statistical Modeling of Program and Read Variability in Resistive Switching Devices,” IEEE International Symposium on Circuits and Systems (ISCAS), 2029 (2014). DOI: 10.1109/ISCAS.2014.6865563
[58] D. Ielmini, ‘Scaling of resistive switching memories,’ SSDM, Tsukuba, Ibaraki, Japan, September 8-11, 2014.
[59] D. Ielmini, S. Balatti and S. Ambrogio, “Stress-induced asymmetric switching and filament instability in electrochemical memories,” ECS Trans. 64, 169-175 (2014). DOI: 10.1149/06408.0169ecst
[60] D. Ielmini, S. Balatti and S. Ambrogio “Scaling of oxide-based resistive switching devices,” Proc. NVMTS, Jeju Island, Korea, October 25-27, 2014. DOI: 10.1109/NVMTS.2014.7060839
[61] D. Ielmini, “Novel applications of phase change materials: from memory to computing,” E/PCOS15, Amsterdam, NL, Sept. 6-8, 2015.
[62] D. Ielmini, “Logic and neuromorphic computing with resistive switches,” Advances in ReRAM: Materials and Interfaces, Hania, Greece, Oct. 11-16, 2015.
[63] D. Ielmini, “Resistive Switching Memories based on Metal Oxides: Mechanisms, Reliability and Scaling,” Semicond. Sci. Technol. 31, 063002 (2016). DOI: 10.1088/0268-1242/31/6/063002

[64] D. Ielmini, S. Ambrogio, V. Milo, S. Balatti, and Z.-Q. Wang, “Neuromorphic computing with hybrid memristive/CMOS synapses for real-time learning,” 2016 IEEE International Symposium Circuits and Systems (ISCAS), Montreal, Canada, May 22-25, 2016. DOI: 10.1109/ISCAS.2016.7527508
[65] N. Ciocchini, M. Laudato, M. Boniardi, E. Varesi, P. Fantini, A. L. Lacaita and D. Ielmini, “Bipolar switching operation in phase change memory devices for high temperature retention,” E/PCOS16, Sept. 4-6, 2016, Cambridge, UK.
[66] D. Ielmini, “Physical Models of Program and Read Fluctuations in Metal Oxide Resistive RAM,” ECS Trans. 75, 4, 19-26 (2016). DOI: 10.1149/07505.0019ecst
[67] M. Laudato, G. Pedretti and D. Ielmini, “Brain-inspired neuromorphic computing with phase change memory (PCM) synapses,” E/PCOS (2017).
[68] D. Ielmini and V. Milo, “Physics-based modeling approaches of resistive switching devices for memory and in-memory computing applications,” J. Computation. Electron. 16(4), 1121-1143 (2017). DOI: 10.1007/s10825-017-1101-9
[69] V. Milo, D. Ielmini, and E. Chicca, “Attractor networks and associative memories with STDP learning in RRAM synapses,” IEDM Tech. Dig. 263-266 (2017). DOI: 10.1109/IEDM.2017.8268369
[70] D. Ielmini, “Brain-inspired computing with resistive switching memory (RRAM): Devices, synapses and neural networks,” Microelectron. Eng. 190, 44-53 (2018). doi:10.1016/j.mee.2018.01.009
[71] V. Milo, G. Pedretti, M. Laudato, A. Bricalli, E. Ambrosi, S. Bianchi, E. Chicca, and D. Ielmini, “Resistive switching synapses for unsupervised learning in feed-forward and recurrent neural networks,” 2018 IEEE International Symposium Circuits and Systems (ISCAS), Firenze, Italy, May 4-7, 2018.
[72] A. Mehonic, A. L. Shluger, D. Gao, I. Valov, E. Miranda, D. Ielmini, A. Bricalli, E. Ambrosi, C. Li, J. J. Yang, Q. Xia, and A. J. Kenyon, “Silicon Oxide (SiO_x) – A Promising Material for Resistance Switching?” Adv. Mater. (2018). Doi: 10.1002/adma.201801187
[73] D. Ielmini and H.-S. P. Wong, “In-memory computing with resistive switching devices,” Nature Electronics 1, 333-343 (2018). doi: 10.1038/s41928-018-0092-2
[74] D. Ielmini, “Calcolo neuromorfico: circuiti elettronici che imitano la mente umana,” Mondo Digitale 79 Dicembre (2018).
[75] D. Ielmini and S. Ambrogio, “Emerging neuromorphic devices,” Nanotechnology 31, 092001 (2019). doi:10.1088/1361-6528/ab554b
[76] V. Milo, G. Malavena, C. Monzio Compagnoni and D. Ielmini, “Memristive and CMOS devices for neuromorphic computing,” Materials, 13, 166 (2020). doi:10.3390/ma13010166
[77] D. Ielmini and G. Pedretti, “Device and circuit architectures for in-memory computing,” Adv. Intell. Syst. 2000040 (2020). doi: 10.1002/aisy.202000040
[78] W. Wang, W. Song, P. Yao, Y. Li, J. Van Nostrand, Q. Qiu, D. Ielmini, J. J. Yang, “Integration and co-design of memristive devices and algorithms for artificial intelligence,” iScience 23, 101809 (2020). doi: 10.1016/j.isci.2020.101809
[79] G. Pedretti, E. Ambrosi and D. Ielmini, “Conductance variations and their impact on the precision of in-memory computing with resistive switching memory (RRAM),” IRPS (2021).
[80] D. Ielmini, Z. Wang, Y. Liu, “Brain-inspired computing via memory device physics,” APL Mater. 9, 050702 (2021); doi: 10.1063/5.0047641
[81] G. Pedretti and D. Ielmini, “In-memory computing with resistive memory circuits: status and outlook,” Electronics 10, 1063 (2021). Doi: 10.3390/electronics10091063
[82] Y.D. Zhao, J.F. Kang and D. Ielmini, “Materials Challenges and Opportunities for Brain-inspired Computing,” MRS Bull. 46, 1 (2021). doi: 10.1557/s43577-021-00205-1
[83] D. V. Christensen, R. Dittmann, B. Linares-Barranco, A. Sebastian, M. Le Gallo, A. Redaelli, S. Slesazeck, T. Mikolajick, S. Spiga, S. Menzel, I. Valov, G. Milano, C. Ricciardi, S.-J. Liang, F. Miao, M. Lanza, T. J. Quill, S. T. Keene, A. Salleo, J. Grollier, D. Marković, A. Mizrahi, P. Yao, J. J. Yang, G. Indiveri, J. P. Strachan, S. Datta, E. Vianello, A. Valentian, J. Feldmann, X. Li, W. H.P. Pernice, H. Bhaskaran, S. Furber, E. Neftci, F. Scherr, W. Maass, S. Ramaswamy, J. Tapson, P. Panda, Y. Kim, G. Tanaka, S. Thorpe, C. Bartolozzi, T. A. Cleland, C. Posch, S.-C. Liu, G. Panuccio, M. Mahmud, A. N. Mazumder, M. Hosseini, T. Mohsenin, E. Donati, S. Tolu, R. Galeazzi, M. E. Christensen, S. Holm, D. Ielmini, N. Pryds, “2022 Roadmap on Neuromorphic Computing and Engineering,” Neuromorphic Computing and Engineering (2022). DOI: https://doi.org/10.1088/2634-4386/ac4a83

International Refereed Journals

[84] G. Ghislotti, D. Ielmini, E. Riedo, M. Martinelli and M. Dellagiovanna, “Picosecond time-resolved luminescence studies of recombination processes in CdTe,” Solid State Commun. 111, 211-216 (1999).
[85] G. Ghislotti, E. Riedo, D. Ielmini and M. Martinelli, “Intersubband relaxation time for $In_xGa_{1-x}As$/AlAs quantum wells with large transition energy,” Appl. Phys. Lett. 75, 3626-3628 (1999).
[86] A. S. Spinelli, A. L. Lacaita, M. Rigamonti, D. Ielmini and G. Ghidini, “Separation of electron and hole traps by transient current analysis,” Microelectron. Eng. 48, 151-154 (1999).
[87] D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Experimental evidence for recombination-assisted leakage in thin oxides,” Appl. Phys. Lett. 76, 1719-1721 (2000).
[88] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, “A recombination model for transient and stationary stress-induced leakage current,” Microelectron. Reliab. 40, 703-706 (2000).
[89] D. Ielmini, A. S. Spinelli, M. A. Rigamonti and A. L. Lacaita, “Modeling of SILC based on electron and hole tunneling - Part I: Transient effects,” IEEE Trans. Electron Devices 47, 1258-1265 (2000).
[90] D. Ielmini, A. S. Spinelli, M. A. Rigamonti and A. L. Lacaita, “Modeling of SILC based on electron and hole tunneling - Part II: Steady-state,” IEEE Trans. Electron Devices 47, 1266-1272 (2000).
[91] D. Ielmini, A. S. Spinelli, M. Beretta and A. L. Lacaita, “Different types of defect in the silicon dioxides characterized by their transient behavior,” J. Appl. Phys. 89, 4189-4191 (2001).
[92] D. Ielmini, A. S. Spinelli, A. L. Lacaita, D. J. DiMaria and G. Ghidini “A Detailed investigation of the quantum yield experiment,” IEEE Trans. Electron Devices 48, 1696-1702 (2001).
[93] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, “A recombination- and trap-assisted tunneling model for stress-induced leakage current,” Solid State Electronics 45, 1361-1369 (2001).

[94] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “A new two-trap tunneling model for the anomalous SILC in flash memories,” Microelectron. Eng. 59, 189-195 (2001).
[95] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “Equivalent cell approach for extraction of the SILC distribution in Flash EEPROM cells,” IEEE Electron Device Lett. 23, 40-42 (2002).
[96] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, “Modeling of stress-induced leakage current and impact ionization in MOS devices,” Solid State Electronics 46, 417-422 (2002).
[97] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Visconti, “Statistical profiling of SILC spot in Flash memories,” IEEE Trans. Electron Devices 49, 1723-1728 (2002).
[98] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “Modeling of anomalous SILC in Flash memories based on tunneling at multiple defects,” Solid State Electronics 46, 1749-1756 (2002).
[99] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “A statistical model for SILC in Flash memories,” IEEE Trans. Electron Devices 49, 1955-1961 (2002).
[100] G. Ghidini, A. Garavaglia, G. Giusto, A. Ghetti, R. Bottini, D. Peschiaroli, M. Scaravaggi, F. Cazzaniga and D. Ielmini, “Impact of gate stack process on conduction and reliability of 0.18um PMOSFET,” Microelectron. Reliab. 43, 1221-1227 (2003).
[101] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita and C. Gerardi, “Study of nanocrystal memory reliability by CAST structures,” Solid-State Electronics 48, 1497-1502 (2004).
[102] D. Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer and R. Bez, “Analysis of phase distribution in phase-change non volatile memories,” IEEE Electron Device Lett. 25, 507-509 (2004).
[103] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “Defect generation statistics in thin gate oxides,” IEEE Trans. Electron Devices 51, 1288-1295 (2004).
[104] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “Impact of correlated generation of oxide defects on SILC and breakdown distributions,” IEEE Trans. Electron Devices 51, 1281-1287 (2004).
[105] A. Redaelli, A. Pirovano, F. Pellizzer, A. L. Lacaita, D. Ielmini and R. Bez, “Electronic switching effect and phase-change transition in chalcogenide materials,” IEEE Electron Device Lett. 25, 684-686 (2004).
[106] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “A comparative study of characterization techniques for oxide reliability in Flash memories,” IEEE Trans. on Device and Material Reliability 4, 320-326 (2004).
[107] G. Puzzilli, D. Caputo, F. Irrera, C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita and C. Gerardi, “Improving floating-gate memory reliability by nanocrystal storage and pulsed tunnel programming,” IEEE Trans. on Device and Material Reliability 4, 390-396 (2004).
[108] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Modeling of tunneling P/E for nanocrystal memories,” IEEE Trans. Electron Devices 52, 569-576 (2005).
[109] R. Gusmeroli, A. S. Spinelli, C. Monzio Compagnoni, D. Ielmini and A. L. Lacaita, “Edge and percolation effects on Vt window in nanocrystal memories,” Microelectronics Engineering 80, 186-189 (2005).
[110] D. Ielmini, D. Mantegazza, A. L. Lacaita, A. Pirovano and F. Pellizzer, “Parasitic reset in the programming transient of phase change memories,” IEEE Electron Device Lett. 26, 799-801 (2005).
[111] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Optimization of threshold voltage window under tunneling program/erase in nanocrystal memories,” IEEE Trans. Electron Devices 52, 2473-2481 (2005).
[112] D. Ielmini, D. Mantegazza, A. L. Lacaita, A. Pirovano and F. Pellizzer, “Switching and programming dynamics in phase change memory cells,” Solid-State Electronics 49, 1826-1832 (2005).
[113] D. Ielmini, A. S. Spinelli and A. Visconti, “Characterization of oxide trap energy by analysis of the SILC roll-off regime in Flash memories,” IEEE Trans. Electron Devices 53, 126-134 (2006).
[114] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Extraction of the floating-gate capacitive-couplings for drain turn-on estimation in discrete-trap memories,” Microelectron. Eng. 83, 319-322 (2006).
[115] D. Ielmini, A. Ghetti, A. S. Spinelli and A. Visconti, “A study of hot hole injection during programming drain disturb in Flash memories,” IEEE Trans. Electron Devices 53, 668-676 (2006).
[116] R. Gusmeroli, A. S. Spinelli, C. Monzio Compagnoni, and D. Ielmini, “Threshold-voltage statistics and conduction regimes in nanocrystal memories,” IEEE Electron Device Lett. 27, 409-411 (2006).
[117] U. Russo, D. Ielmini, A. Redaelli and A. L. Lacaita, “Intrinsic data retention in nanoscaled phase-change memories - Part I: Monte Carlo model for crystallization and percolation,” IEEE Trans. Electron Devices 53, 3032-3039 (2006).
[118] A. Redaelli, D. Ielmini, U. Russo and A. L. Lacaita, “Intrinsic data retention in nanoscaled phase-change memories - Part II: Statistical analysis and prediction of failure time,” IEEE Trans. Electron Devices 53, 3040-3046 (2006).
[119] D. Ielmini, A. L. Lacaita and D. Mantegazza, “Recovery and drift dynamics of resistance and threshold voltages in phase change memories,” IEEE Trans. Electron Devices 54, 308-315 (2007).
[120] D. Ielmini and Y. Zhang, “Evidence for trap-limited transport in the subthreshold conduction regime of chalcogenide glasses,” Appl. Phys. Lett. 90, 192102 (2007).
[121] D. Ielmini and Y. Zhang, “Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices,” J. Appl. Phys. 102, 054517 (2007).
[122] U. Russo, D. Ielmini and A. L. Lacaita, “Analytical modeling of chalcogenide crystallization for PCM data-retention extrapolation,” IEEE Trans. Electron Devices 54, 2769-2777 (2007).
[123] D. Mantegazza, D. Ielmini, A. Pirovano and A. L. Lacaita “Anomalous cells with low resistance in phase change memory arrays,” IEEE Electron Device Lett. 28, 865-867 (2007).
[124] U. Russo, D. Ielmini, A. Redaelli and A. L. Lacaita, “Modeling of programming and read performance in phase-change memories - Part I: Cell optimization and scaling,” IEEE Trans. Electron Devices 55, 506-514 (2008).
[125] U. Russo, D. Ielmini, A. Redaelli and A. L. Lacaita, “Modeling of programming and read performance in phase-change memories – Part II: program disturb and mixed scaling approach,” IEEE Trans. Electron Devices 55, 515-522 (2008).
[126] A. Redaelli, A. Pirovano, I. Tortorelli, D. Ielmini and A. L. Lacaita “A reliable technique for experimental evaluation of crystallization activation energy in PCMs,” IEEE Electron Device Lett. 29, 41-43 (2008).
[127] D. Mantegazza, D. Ielmini, A. Pirovano, A. L. Lacaita, E. Varesi, F. Pellizzer and R. Bez, “Explanation of programming distributions in phase-change memory arrays based on crystallization time statistics,” Solid-State Electronics. 52, 584-590 (2008).

[128] A. Redaelli, D. Ielmini, U. Russo and A. L. Lacaita “Modeling and simulation of conduction characteristics and programming operation in nanoscaled phase-change memory cells,” J. Computational and Theoretical Nanoscience 5, 1183-1191 (2008).
[129] D. Ielmini, D. Mantegazza and A. L. Lacaita, “Voltage controlled relaxation oscillations in phase-change memory devices,” IEEE Electron Device Lett. 30, 568-570 (2008).
[130] D. Ielmini, S. Lavizzari, D. Sharma and A. L. Lacaita, “Temperature acceleration of structural relaxation in $Ge_2Sb_2Te_5$,” Appl. Phys. Lett. 92, 193511 (2008).
[131] D. Ielmini, “Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses,” Phys. Rev. B 78, 035308 (2008).
[132] A. L. Lacaita, D. Ielmini and D. Mantegazza, “Status and challenges of phase change memory modeling,” Solid-State Electronics 52, 1443-1451 (2008).
[133] U. Russo, D. Ielmini, C. Cagli and A. L. Lacaita, “Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices,” IEEE Trans. Electron Devices 56, 186-192 (2009). DOI: 10.1109/TED.2008.2010583
[134] U. Russo, D. Ielmini, C. Cagli and A. L. Lacaita, “Self-accelerated thermal dissolution model for reset programming in NiO-based resistive switching memory (RRAM) devices,” IEEE Trans. Electron Devices 56, 193-200 (2009).
[135] M. Boniardi, A. Redaelli, A. Pirovano, I. Tortorelli, D. Ielmini and F. Pellizzer, “A physics-based model of electrical conduction decrease with time in amorphous $Ge_2Sb_2Te_5$,” J. Appl. Phys. 105, 084506 (2009).
[136] U. Russo, D. Kalamanathan, D. Ielmini, A. L. Lacaita and M. Kozicki, “Study of multilevel programming in programmable metallization cell (PMC) memory,” IEEE Trans. Electron Devices 56,1040-1047 (2009). DOI: 10.1109/TED.2009.2016019
[137] D. Ielmini, C. Cagli and F. Nardi, “Resistance transition in metal oxides induced by electronic threshold switching,” Appl. Phys. Lett. 94, 063511 (2009).
[138] D. Ielmini and M. Boniardi, “Common signature of many-body thermal excitation in structural relaxation and crystallization of chalcogenide glasses,” Appl. Phys. Lett. 94, 091906 (2009).
[139] D. Ielmini, M. Boniardi, A. L. Lacaita, A. Redaelli and A. Pirovano, “Unified mechanisms for structure relaxation and crystallization in phase-change memory,” Microelectron. Eng. 86, 1942-1945 (2009).
[140] D. Ielmini, D. Sharma, S. Lavizzari and A. L. Lacaita, “Reliability impact of chalcogenide-structure relaxation in phase change memory (PCM) cells – Part I: Experimental study,” IEEE Trans. Electron Devices 56, 1070-1077 (2009).
[141] S. Lavizzari, D. Ielmini, D. Sharma and A. L. Lacaita, “Reliability impact of chalcogenide-structure relaxation in phase change memory (PCM) cells – Part II: Physics-based modeling,” IEEE Trans. Electron Devices 56, 1078-1085 (2009).
[142] D. Kamalanathan, U. Russo, D. Ielmini, and M. N. Kozicki, “Voltage-driven ON-OFF transition and tradeoff with program and erase current in programmable metallization cell (PMC) memory,” IEEE Electron Device Lett. 30, 553-555 (2009).
[143] D. Ielmini and F. Gattel, “Delay correction for accurate extraction of time exponent and activation energy of NBTI,” IEEE Electron Device Lett. 30, 684-686 (2009).
[144] C. Cagli, F. Nardi and D. Ielmini, ”Modeling of set/reset operations in NiO-based resistive-switching memory (RRAM) devices,” IEEE Trans. Electron Devices 56, 1712-1720 (2009).
[145] D. Ielmini, M. Manigrasso, F. Gattel and G. Valentini, “A new NBTI model based on hole trapping and structure relaxation in MOS dielectrics,” IEEE Trans. Electron Devices 56, 1943-1952 (2009).
[146] U. Russo, C. Cagli, S. Spiga, E. Cianci and D. Ielmini, “Impact of electrode materials on resistive-switching memory (RRAM) programming,” IEEE Electron Device Lett. 30, 817-819 (2009).
[147] D. Ielmini, F. Nardi, C. Cagli and A. L. Lacaita, “Size-dependent retention time in NiO-based resistive switching memories,” IEEE Electron Device Lett. 31, 353-355 (2010).
[148] D. Ielmini, F. Nardi and C. Cagli, “Resistance-dependent amplitude of random telegraph signal noise in resistive switching memories,” Appl. Phys. Lett. 96, 053503 (2010).
[149] D. Mantegazza, D. Ielmini and A. L. Lacaita, “Incomplete filament crystallization during set operation in PCM cells,” IEEE Electron Device Lett. 31, 341-343 (2010).
[150] S. Lavizzari, D. Sharma and D. Ielmini, “Threshold-switching delay controlled by 1/f current fluctuations in phase-change memory devices,” IEEE Trans. Electron Devices 57, 1047-1054 (2010).
[151] D. Ielmini, “Reset-set instability in unipolar resistive switching memory,” IEEE Electron Device Lett. 31, 552-554 (2010).
[152] S. Lavizzari, D. Ielmini and A. L. Lacaita, “A new transient model for recovery and relaxation oscillations in phase change memories,” IEEE Trans. Electron Devices 57, 1838-1845 (2010).
[153] A. Calderoni, M. Ferro, D. Ielmini and P. Fantini “A unified hopping model for sub-threshold current of Phase Change Memories in amorphous state”, IEEE Electron Device Lett. 31, 1023-1025 (2010).
[154] M. Boniardi, D. Ielmini, S. Lavizzari, A. L. Lacaita, A. Redaelli and A. Pirovano, “Statistics of resistance drift due to structural relaxation in phase-change memory arrays,” IEEE Trans. Electron Devices 57, 2690-2696 (2010).
[155] S. Lavizzari, D. Ielmini and A. L. Lacaita, “Transient simulation of delay and switching effects in phase change memories,” IEEE Trans. Electron Devices 57, 3257-3264 (2010).
[156] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, D. J. Wouters, “Control of filament size and reduction of reset current below 10 μA in NiO resistance switching memories,” Solid State Electronics 58, 42-47 (2011).
[157] M. Boniardi, D. Ielmini, I. Tortorelli, A. Redaelli, A. Pirovano, M. Allegra, M. Magistretti, C. Bresolin, D. Erbetta, A. Modelli, E. Varesi, F. Pellizzer, A. L. Lacaita and R. Bez, “Impact of Ge–Sb–Te compound engineering on the set operation performance in phase-change memories,” Solid State Electronics 58, 11-16 (2011).
[158] D. Ielmini, S. Spiga, F. Nardi, C. Cagli, A. Lamperti, E. Cianci, and M. Fanciulli, “Scaling analysis of submicrometer nickel-oxide-based resistive switching memory devices,” J. Appl. Phys. 109, 034506 (2011).
[159] S. Larentis, C. Cagli, F. Nardi and D. Ielmini, “Filament diffusion model for simulating reset and retention processes in RRAM,” Microelectron. Eng. 88, 1119-1123 (2011). DOI: 10.1016/j.mee.2011.03.055
[160] D. Ielmini, C. Cagli and F. Nardi, “Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories,” Nanotechnology 22, 254022 (2011). DOI: 10.1088/0957-4484/22/25/254022
[161] F. Nardi, C. Cagli, S. Spiga and D. Ielmini, “Reset instability in pulsed-operated unipolar resistive switching memory,” IEEE Electron Device Lett. 32, 719-721 (2011).

[162] M. Boniardi and D. Ielmini, “Physical origin of the resistance drift exponent in amorphous phase change materials,” Appl. Phys. Lett. 98, 243506 (2011).
[163] D. Ielmini, F. Nardi and C. Cagli, “Universal reset characteristics of unipolar and bipolar metal-oxide RRAM,” IEEE Trans. Electron Devices 58, 3246-3253 (2011). DOI: 10.1109/TED.2011.2161088
[164] C. Cagli, F. Nardi, B. Harteneck, Z. Tan, Y. Zhang, and D. Ielmini, “Resistive-switching crossbar memory based on Ni-NiO core-shell nanowires,” Small 7, 2899-2905 (2011). Inside cover issue. DOI: 10.1002/smll.201101157
[165] D. Ielmini, “Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth,” IEEE Trans. Electron Devices 58, 4309-4317 (2011). DOI: 10.1109/TED.2011.2167513
[166] S. Long, C. Cagli, D. Ielmini, M. Liu and J. Suñé, “Reset Statistics of NiO-Based Resistive Switching Memories,” IEEE Electron Device Lett. 32, 1570-1572 (2011). DOI: 10.1109/LED.2011.2163613
[167] M. Rizzi, A. Spessot, P. Fantini and D. Ielmini, “Role of mechanical stress in the resistance drift of $Ge_2Sb_2Te_5$ films and phase change memories,” Appl. Phys. Lett. 99, 223513 (2011). Selected for the December 12, 2011 issue of Virtual Journal of Nanoscale Science & Technology (AIP and APS).
[168] S. Long, C. Cagli, D. Ielmini, M. Liu, and J. Suñé, “Analysis and modeling of resistive switching statistics,” J. Appl. Phys. 111, 074508 (2012). DOI: 10.1063/1.3699369
[169] S. Choi, S. Balatti, F. Nardi, and D. Ielmini, “Size-dependent drift of resistance due to surface defect relaxation in conductive-bridge memory,” IEEE Electron Device Lett. 33, 1189–1191 (2012). DOI: 10.1109/LED.2012.2199074
[170] D. Ielmini, F. Nardi and S. Balatti, “Evidence for voltage driven set/reset processes in bipolar switching RRAM,” IEEE Trans. Electron Devices 59, 2049–2056 (2012). DOI: 10.1109/TED.2012.2199497
[171] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer and D. Ielmini, “Resistive switching by voltage-driven ion migration in bipolar RRAM – Part I: Experimental study,” IEEE Trans. Electron Devices 59, 2461–2467 (2012). DOI: 10.1109/TED.2012.2202319
[172] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer and D. Ielmini, “Resistive switching by voltage-driven ion migration in bipolar RRAM – Part II: Modeling,” IEEE Trans. Electron Devices 59, 2468–2475 (2012). DOI: 10.1109/TED.2012.2202320
[173] A. Calderoni, M. Ferro, E. Varesi, P. Fantini, M. Rizzi, and D. Ielmini, “Understanding Over-Reset Transition in Phase Change Memory (PCM) Characteristics,” IEEE Electron Device Lett. 33, 1267–1269 (2012).
[174] N. Ciocchini, M. Cassinerio, D. Fugazza and D. Ielmini, “Modeling of threshold voltage drift in phase change memory (PCM) devices,” IEEE Trans. Electron Devices 59, 3084-3090 (2012). DOI: 10.1109/TED.2012.2214784
[175] F. Nardi, D. Deleruyelle, S. Spiga, C. Muller, B. Bouteille and D. Ielmini, “Switching of nanosized filaments in NiO by conductive atomic force microscopy,” J. Appl. Phys. 112, 064310 (2012). DOI: 10.1063/1.4752032
[176] E. Piccinini, A. Cappelli, F. Buscemi, R. Brunetti, D. Ielmini, M. Rudan, and C. Jacoboni, “Hot-carrier trap-limited transport in switching chalcogenides,” J. Appl. Phys. 112, 083722 (2012). DOI: 10.1063/1.4761997
[177] F. Nardi, S. Balatti, S. Larentis, D. C. Gilmer and D. Ielmini, “Complementary switching in oxide-based bipolar resistive switching memory (RRAM),” IEEE Trans. Electron Devices 60, 70-77 (2013). DOI: 10.1109/TED.2012.2226728
[178] D. Ielmini, C. Cagli, F. Nardi, and Y. Zhang, “Nanowire-based resistive switching memories: devices, operation and scaling,” J. Phys. D: Appl. Phys. 46, 074006 (2013). DOI:10.1088/0022-3727/46/7/074006. This article was selected for inclusion in the exclusive ‘Highlights of 2013’ collection of the J. Phys. D: Applied Physics. Articles are chosen on the basis of referee endorsement, novelty, scientific impact and broadness of appeal.
[179] S. Balatti, S. Larentis, D. Gilmer and D. Ielmini, “Multiple memory states in resistive switching devices through controlled size and orientation of the conductive filament,” Adv. Mater. 25, 1474–1478 (2013). DOI: 10.1002/adma.201204097
[180] D. Ielmini, S. Balatti, and S. Larentis, “Filament evolution during set and reset transitions in oxide resistive switching memory (RRAM),” Jpn. J. Appl. Phys. 52, 04CD10 (2013). DOI: 10.7567/JJAP.52.04CD10
[181] F. Xiong, M.-H. Bae, Y. Dai, A. D. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini and E. Pop, “Self-Aligned Nanotube-Nanowire Phase Change Memory,” Nano Lett. 13, 464–469 (2013). DOI: 10.1021/nl3038097
[182] S. Ambrogio, S. Balatti, F. Nardi, S. Facchinetti, and D. Ielmini, “Spike-timing dependent plasticity in a transistor-selected resistive switching memory,” Nanotechnology 24, 384012 (2013). DOI: 10.1088/0957-4484/24/38/384012
[183] S. Balatti, S. Ambrogio, D. C. Gilmer, and D. Ielmini, “Set variability and failure induced by complementary switching in bipolar RRAM,” IEEE Electron Device Lett. 34, 861-863 (2013). DOI: 10.1109/LED.2013.2261451
[184] M. Cassinerio, N. Ciocchini, and D. Ielmini, “Evidence for electrically induced drift of threshold voltage in $Ge_2Sb_2Te_5$,” Appl. Phys. Lett. 103, 023502 (2013). DOI: 10.1063/1.4811553.
[185] M. Cassinerio, N. Ciocchini, and D. Ielmini, “Logic computation in phase change materials by threshold and memory switching,” Adv. Mater. 25, 5975–5980 (2013). DOI: 10.1002/adma.201301940
[186] M. Rizzi, M. Ferro, P. Fantini, and D. Ielmini, “Energy Landscape Model of Conduction and Phase Transition in Phase Change Memories,” IEEE Trans. Electron Devices 60, 3618-3624 (2013). DOI: 10.1109/TED.2013.2280791
[187] N. Ciocchini, M. Cassinerio, D. Fugazza, and D. Ielmini, “Evidence for Non-Arrhenius Kinetics of Crystallization in Phase Change Memory Devices,” IEEE Trans. Electron Devices 60, 3767-3774 (2013). DOI: 10.1109/TED.2013.2282637
[188] S. Ambrogio, S. Balatti, S. Choi and D. Ielmini, “Impact of the mechanical stress on switching characteristics of electrochemical resistive memory,” Adv. Mater. 26, 3885–3892 (2014). DOI: 10.1002/adma.201306250
[189] N. Ciocchini, E. Palumbo, M. Borghi, P. Zuliani, R. Annunziata, D. Ielmini, “Modeling resistance instabilities of set and reset states in phase change memory with Ge-rich GeSbTe,” IEEE Trans. Electron Devices 61, 2136-2144 (2014). DOI: 10.1109/TED.2014.2313889
[190] K. V. Mitrofanov, A. V. Kolobov, P. Fons, X. Wang, J. Tominaga, Y. Tamenori, T. Uruga, N. Ciocchini, and D. Ielmini, “Ge L3-edge x-ray absorption near-edge structure study of structural changes accompanying conductivity drift in the amorphous phase of $Ge_2Sb_2Te_5$,” J. Appl. Phys. 115, 173501 (2014). DOI: 10.1063/1.4874415
[191] S. Ambrogio, S. Balatti, D. C. Gilmer, and D. Ielmini, “Analytical modeling of oxide-based bipolar resistive memories and complementary resistive switches,” IEEE Trans. Electron Devices 61, 2378-2386 (2014). DOI: 10.1109/TED.2014.2325531
[192] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, “Statistical fluctuations in HfO_x resistive-switching memory (RRAM): Part I – Set/Reset variability,” IEEE Trans. Electron Devices 61, 2912-2919 (2014). DOI: 10.1109/TED.2014.2330200

[193] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Statistical fluctuations in HfO_x resistive-switching memory (RRAM): Part II – Random telegraph noise," IEEE Trans. Electron Devices 61, 2920-2927 (2014). DOI: 10.1109/TED.2014.2330202
[194] Z.-Q. Wang, S. Ambrogio, S. Balatti and D. Ielmini, "A 2-transistor/1-resistor artificial synapse capable of communication and stochastic learning for neuromorphic systems," Front. Neurosci. 8:438 (2015). DOI: 10.3389/fnins.2014.00438
[195] N. Ciocchini and D. Ielmini, "Pulse-induced crystallization in phase change memories under set and disturb conditions," IEEE Trans. Electron Devices 62, 847-854 (2015). DOI: 10.1109/TED.2015.2389895
[196] Y.-M. Koo, S. Ambrogio, J. Woo, J. Song, D. Ielmini, and H. Hwang, "Accelerated Retention Test Method by Controlling Ion Migration Barrier of ReRAM," IEEE Electron Device Lett. 36, 238-240 (2015). DOI: 10.1109/LED.2015.2394302
[197] S. Balatti, S. Ambrogio, Z.-Q. Wang, and D. Ielmini, "True random number generation by variability of resistive switching in oxide-based devices," IEEE J. Emerging Topics in Circuits and Systems (JETCAS) 5, 214-221 (2015). DOI: 10.1109/JETCAS.2015.2426492
[198] S. Balatti, S. Ambrogio, and D. Ielmini, "Normally-off logic based on resistive switches – Part I: Logic gates," IEEE Trans. Electron Devices 62, 1831-1838 (2015). DOI: 10.1109/TED.2015.2422999
[199] S. Balatti, S. Ambrogio, and D. Ielmini, "Normally-off logic based on resistive switches – Part II: Logic circuits," IEEE Trans. Electron Devices 62, 1839-1847 (2015). DOI: 10.1109/TED.2015.2423001
[200] M. Rizzi, N. Ciocchini, A. Montefiori, M. Ferro, P. Fantini, A. L. Lacaita, and D. Ielmini, "Cell-to-Cell and Cycle-to-Cycle Retention Statistics in Phase-Change Memory Arrays," IEEE Trans. Electron Devices 62, 2205–2211 (2015). DOI: 10.1109/TED.2015.2434278
[201] S. Balatti, S. Ambrogio, Z.-Q. Wang, S. Sills, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Voltage-controlled cycling endurance of HfO_x-based resistive-switching memory (RRAM)," IEEE Trans. Electron Devices 62, 3365-3372 (2015). DOI: 10.1109/TED.2015.2463104
[202] N. Ciocchini, M. Laudato, A. Leone, P. Fantini, A. L. Lacaita, and D. Ielmini, "Impact of thermoelectric effects on phase change memory (PCM) characteristics," IEEE Trans. Electron Devices 62, 3264-3271 (2015). DOI: 10.1109/TED.2015.2465835
[203] S. Ambrogio, S. Balatti, V. McCaffrey, D. Wang, and D. Ielmini, "Noise-induced resistance broadening in resistive switching memory (RRAM) - Part I: Intrinsic cell behavior," IEEE Trans. Electron Devices 62, 3805-3811 (2015). DOI: 10.1109/TED.2015.2475598
[204] S. Ambrogio, S. Balatti, V. McCaffrey, D. Wang, and D. Ielmini, "Noise-induced resistance broadening in resistive switching memory (RRAM) - Part II: Array statistics," IEEE Trans. Electron Devices 62, 3812-3819 (2015). DOI: 10.1109/TED.2015.2477135
[205] S. Ambrogio, S. Balatti, V. Milo, R. Carboni, Z. Wang, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Neuromorphic learning and recognition with one-transistor-one-resistor synapses and bistable metal oxide RRAM," IEEE Trans. Electron Devices 63, 1508-1515 (2016). DOI: 10.1109/TED.2016.2526647
[206] S. Ambrogio, N. Ciocchini, M. Laudato, V. Milo, A. Pirovano, P. Fantini and D. Ielmini, "Unsupervised learning by spike timing dependent plasticity in phase change memory (PCM) synapses," Front. Neurosci. 10:56 (2016). DOI: 10.3389/fnins.2016.00056
[207] S. Balatti, S. Ambrogio, R. Carboni, V. Milo, Z.-Q. Wang, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Physical unbiased generation of random numbers with coupled resistive switching devices," IEEE Trans. Electron Devices 63, 2029-2035 (2016). DOI: 10.1109/TED.2016.2537792
[208] N. Ciocchini, M. Laudato, M. Boniardi, E. Varesi, P. Fantini, A. L. Lacaita, and D. Ielmini, "Bipolar switching in chalcogenide phase change memory," Sci. Rep. 6, 29162 (2016). DOI: 10.1038/srep29162
[209] S. Ambrogio V. Milo, Z. Wang, S. Balatti, and D. Ielmini, "Analytical modeling of current overshoot in oxide-based resistive switching memory (RRAM)," IEEE Electron Device Lett. 37, 1268-1271 (2016). DOI: 10.1109/LED.2016.2600574
[210] Z. Wang, S. Ambrogio, S. Balatti, S. Sills, A. Calderoni, N. Ramaswamy, D. Ielmini, "Post-cycling degradation in metal-oxide bipolar resistive switching memory (RRAM)," IEEE Trans. Electron Devices 63, 4279-4287 (2016). DOI: 10.1109/TED.2016.2604370
[211] G. Pedretti, V. Milo, S. Ambrogio, R. Carboni, S. Bianchi, A. Calderoni, N. Ramaswamy, A. S. Spinelli, D. Ielmini, "Memristive neural network for on-line learning and tracking with brain-inspired spike timing dependent plasticity," Sci. Rep. 7:5288 (2017). DOI: 10.1038/s41598-017-05480-0
[212] G. Pedretti, V. Milo, S. Ambrogio, R. Carboni, S. Bianchi, A. Calderoni, N. Ramaswamy, A. S. Spinelli, D. Ielmini, "Stochastic learning in neuromorphic hardware via spike timing dependent plasticity with RRAM synapses," IEEE J. Emerging Topics in Circuits and Systems (JETCAS) 8, 77-85 (2018). DOI: 10.1109/JETCAS.2017.2773124
[213] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "Resistive switching device technology based on silicon oxide for improved on-off ratio – Part I: Memory devices," IEEE Trans. Electron Devices 65, 115-121 (2018). DOI: 10.1109/TED.2017.2777986
[214] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "Resistive switching device technology based on silicon oxide for improved on-off ratio – Part II: Select devices," IEEE Trans. Electron Devices 65, 122-128 (2018). DOI: 10.1109/TED.2017.2776085
[215] Y. Ren, V. Milo, Z. Wang, H. Xu, D. Ielmini, X. Zhao, Y. Liu, "Analytical modeling of organic−inorganic $CH_3NH_3PbI_3$ perovskite resistive switching and its application for neuromorphic recognition," Adv. Theory Simul. 1, 1700035 (2018). DOI: 10.1002/adts.201700035
[216] V. Milo, G. Pedretti, R. Carboni, A. Calderoni, N. Ramaswamy, S. Ambrogio, and D. Ielmini, "A 4-transistors/one-resistor hybrid synapse based on resistive switching memory (RRAM) capable of spike-rate dependent plasticity (SRDP)," IEEE Trans. VLSI 26, 2806-2815 (2018). DOI: 10.1109/TVLSI.2018.2818978
[217] R. Carboni, S. Ambrogio, W. Chen, M. Siddik, J. Harms, A. Lyle, W. Kula, G. Sandhu and D. Ielmini, "Modeling of breakdown-limited endurance in spin-transfer torque (STT) magnetic memory under pulsed cycling regime," IEEE Trans. Electron Devices 65, 2470-2478 (2018). DOI: 10.1109/TED.2018.2822343
[218] R. Carboni, W. Chen, M. Siddik, J. Harms, A. Lyle, W. Kula, G. Sandhu and D. Ielmini, "Random number generation by differential read of stochastic switching in spin-transfer torque memory," IEEE Electron Device Lett. 39, 951-954 (2018). DOI: 10.1109/LED.2018.2833543

[219] M. Lanza, H.-S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. C. Regan, L. Larcher, M. A. Villena, J. J. Yang, L. Goux, A. Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. Magyari-Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T.-H. Hou, B. Hudec, D. Akinwande, R. Ge, S. Ambrogio, J. B. Roldan, E. Miranda, J. Suñe, K. L. Pey, X. Wu, N. Raghavan, E. Wu, W. D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui, Y. Shi, "Recommended methods to study resistive switching devices," Adv. Electronic Materials 5, 1800143 (2019). doi: 10.1002/aelm.201800143

[220] M. Wang, W. Wang, W. R. Leow, C. Wan, G. Chen, Y. Zeng, J. Yu, Y. Liu, P. Cai, H. Wang, D. Ielmini, and X. Chen, "Enhancing the Matrix Addressing of Flexible Sensory Arrays by a Highly Nonlinear Threshold Switch," Adv. Mater. 1802516 (2018). DOI: 10.1002/adma.201802516

[221] Z. Sun, E. Ambrosi, A. Bricalli and D. Ielmini, "Logic computing with stateful neural networks of resistive switches," Adv. Mater. 30 1802554 (2018). Doi: 10.1002/adma.201802554

[222] W. Wang, G. Pedretti, V. Milo, R. Carboni, A. Calderoni, N. Ramaswamy, A. S. Spinelli, and D. Ielmini, "Learning of spatio-temporal patterns in a spiking neural network with resistive switching synapses," Science Advances 4, 9, eaat475 (2018). DOI: 10.1126/sciadv.aat4752

[223] E. Ambrosi, A. Bricalli, M. Laudato and D. Ielmini, "Impact of oxide and electrode materials on the switching characteristics of oxide ReRAM devices," Faraday Discussions 213, 87-98 (2019). DOI: 10.1039/c8fd00106e

[224] W. Wang, M. Wang, E. Ambrosi, A. Bricalli, M. Laudato, Z. Sun, X. Chen and D. Ielmini, "Surface diffusion-limited lifetime of silver/copper nanofilaments in resistive switching devices," Nature Communications 10:81 (2019). Doi: 10.1038/s41467-018-07979

[225] Z. Sun, G. Pedretti, E. Ambrosi, A. Bricalli, W. Wang and D. Ielmini, "Solving matrix equations in one step with crosspoint resistive arrays," PNAS 116 (10) 4123-4128 (2019). doi/10.1073/pnas.1815682116

[226] I. Muñoz-Martín, S. Bianchi, G. Pedretti, O. Melnic, S. Ambrogio, and D. Ielmini, "Unsupervised learning to overcome catastrophic forgetting in neural networks," IEEE Journal of Exploratory Solid-State Computational Devices and Circuits 5, 58-66 (2019). Doi: 10.1109/JXCDC.2019.2911135

[227] R. Carboni, D. Ielmini, "Stochastic Memory Devices for Security and Computing," Adv. Electron. Mater. 1900198 (2019). Doi: 10.1002/aelm.201900198

[228] W. Wang, M. Laudato, E. Ambrosi, A. Bricalli, E. Covi, Y.-H. Lin, and D. Ielmini, "Volatile Resistive Switching Memory Based on Ag Ion Drift/Diffusion – Part I: Numerical Modeling Compact Modeling," IEEE Trans. Electron Devices 66, 3795 - 3801 (2019). DOI: 10.1109/TED.2019.2928890

[229] W. Wang, M. Laudato, E. Ambrosi, A. Bricalli, E. Covi, Y.-H. Lin, and D. Ielmini, "Volatile Resistive Switching Memory Based on Ag Ion Drift/Diffusion – Part II: Compact Modeling," IEEE Trans. Electron Devices 66, 3802 - 3808 (2019). Doi: 10.1109/TED.2019.2928888

[230] V. Milo, C. Zambelli, P. Olivo, E. Pérez, M. K. Mahadevaiah, O. G. Ossorio, Ch. Wenger, and D. Ielmini, "Multilevel HfO_2-based RRAM devices for low-power neuromorphic networks," APL Mater. 7, 081120 (2019). doi: 10.1063/1.5108650

[231] R. Carboni, E. Vernocchi, M. Siddik, J. Harms, A. Lyle, G. Sandhu and D. Ielmini, "A physics-based compact model of stochastic switching in spin-transfer torque magnetic memory," IEEE Trans. Electron Devices 66, 4176 – 4182 (2019). DOI: 10.1109/TED.2019.2933315

[232] Y. Ren, Y. Tao, X. Li, Z. Wang, H. Xu, D. Ielmini, Y. Lin, X. Zhao, Y. Liu, "Analytical Modeling of Electrochemical Metallization Memory Device with Dual-layer structure of Ag/AgInSbTe/Amorphous C/Pt", Semiconductor Science and Technology 35 02LT01 (2019). Doi: 10.1088/1361-6641/ab5d94

[233] G. Pedretti, P. Mannocci, S. Hashemkhani, V. Milo, O. Melnic, E. Chicca, and D. Ielmini, "A spiking recurrent neural network with phase change memory neurons and synapses for the accelerated solution of constraint satisfaction problems," IEEE Journal of Exploratory Solid-State Computational Devices and Circuits 6, 89-97 (2019). Doi: 10.1109/JXCDC.2020.2992691

[234] Z. Sun, G. Pedretti, A. Bricalli, D. Ielmini, "One-step regression and classification with crosspoint resistive memory arrays," Sci. Adv. 6:eaay2378 (2020). DOI: 10.1126/sciadv.aay2378

[235] Z. Sun, E. Ambrosi, G. Pedretti, A. Bricalli, and D. Ielmini, "In-memory PageRank Accelerator with a Crosspoint Array of Resistive Memories," IEEE Trans. Electron Devices 67, 1466 – 1470 (2020). Doi: 10.1109/TED.2020.2966908

[236] Z. Wang, T. Zeng, Y. Ren, Y. Lin, H. Xu, X. Zhao, Y. Liu and D. Ielmini, "Toward a generalized Bienenstock-Cooper-Munro rule for spatiotemporal learning via triplet-STDP in memristive devices," Nature Communications 11:1510 (2020). Doi: 10.1038/s41467-020-15158-3

[237] S. Bianchi, I. Munoz, D. Ielmini, "Bio-inspired techniques in a fully digital approach for lifelong learning," Front. Neurosci. 14:379 (2020). doi: 10.3389/fnins.2020.00379

[238] Z. Sun, G. Pedretti, E. Ambrosi, A. Bricalli, and D. Ielmini, "In-memory eigenvector computation in time O(1)," Adv. Intell. Sys. 2, 2000042 (2020). doi: 10.1002/aisy.202000042

[239] Z. Sun, G. Pedretti, P. Mannocci, E. Ambrosi, A. Bricalli, and D. Ielmini, "Time complexity of in-memory solution of linear systems," IEEE Trans. Electron Devices 67, 2945-2951 (2020). Doi: 10.1109/TED.2020.2992435

[240] S. Bianchi, G. Pedretti, I. Muñoz-Martín, A. Calderoni, N. Ramaswamy, S. Ambrogio, and D. Ielmini, "A compact model for stochastic spike-timing-dependent plasticity (STDP) based on resistive switching memory (RRAM) synapses," IEEE Trans. Electron Devices 67, 2800-2806 (2020). Doi: 10.1109/TED.2020.2992386

[241] G. Milano, G. Pedretti, M. Fretto, L. Boarino, F. Benfenati, D. Ielmini, I. Valov and C. Ricciardi, "Brain-Inspired Structural Plasticity through Reweighting and Rewiring in Multi-Terminal Self-Organizing Memristive Nanowire Networks," Adv. Intell. Syst. 2, 2000096 (2020). doi: 10.1002/aisy.202000096

[242] T. Zanotti, C. Zambelli, F. M. Puglisi, V. Milo, E. Perez, M. K. Mahadevaiah, O. G. Ossorio, C. Wenger, P. Pavan, P. Olivo, and D. Ielmini, "Reliability of Logic-in-Memory Circuits in Resistive Memory Arrays," IEEE Trans. Electron Devices 67, 4611-4615 (2020). doi: 10.1109/TED.2020.3025271

[243] W. Wang, E. Covi, A. Milozzi, M. Farronato, S. Ricci, C. Sbandati, G. Pedretti, and D. Ielmini, "Neuromorphic motion detection and orientation selectivity by volatile resistive switching memories," Advanced Intelligent Systems 3, 2000224 (2020). doi: 10.1002/aisy.202000224

[244] C. Lammie, M. Rahimi Azghadi, and D. Ielmini, "Empirical metal-oxide RRAM device endurance and retention model for deep learning simulations" Semicond. Sci. Technol. (2021). Doi: 10.1088/1361-6641/abf29d

[245] V. Milo, A. Glukhov, E. Perez, C. Zambelli, N. Lepri, M. K. Mahadevaiah, E. Perez-Bosch Quesada, P. Olivo, C. Wenger, and D. Ielmini, "Accurate program/verify schemes of resistive switching memory (RRAM) for in-memory neural network circuits," IEEE Trans. Electron Devices 68, 3832-3837 (2021). Doi: 10.1109/TED.2021.3089995

[246] G. Pedretti, P. Mannocci, C. Li, Z. Sun, J. P. Strachan, and D. Ielmini, "Redundancy and analogue slicing for precise in-memory machine learning - Part I: Programming techniques," IEEE Trans. Electron Devices 68, 4373-4378 (2021). doi: 10.1109/TED.2021.3095433.

[247] G. Pedretti, P. Mannocci, C. Li, Z. Sun, J. P. Strachan, and D. Ielmini, "Redundancy and analogue slicing for precise in-memory machine learning - Part II: Applications and benchmark," IEEE Trans. Electron Devices 68, 4379-4383 (2021). doi: 10.1109/TED.2021.3095430.

[248] E. Covi, W. Wang, Y.-H. Lin, M. Farronato, E. Ambrosi, and D. Ielmini, "Switching Dynamics of Ag based Filamentary Volatile Resistive Switching Devices – Part I: Experimental Characterization," IEEE Trans. Electron Devices 68, 4335-4341 (2021). DOI: 10.1109/TED.2021.3076029

[249] W. Wang, E. Covi, Y.-H. Lin, E. Ambrosi, A. Milozzi, C. Sbandati, M. Farronato, and D. Ielmini, "Switching Dynamics of Ag based Filamentary Volatile Resistive Switching Devices – Part II: Mechanism and Modeling," IEEE Trans. Electron Devices 68, 4342-4349 (2021). DOI: 10.1109/TED.2021.3095033

[250] I. Munoz-Martin, S. Bianchi, S. Hashemkhani, G. Pedretti, O. Melnic, and D. Ielmini, "A brain-inspired homeostatic neuron based on phase-change memories for efficient neuromorphic computing," Front. Neurosci. 15:709053 (2021). doi: 10.3389/fnins.2021.709053

[251] G. Milano, G. Pedretti, K. Montano, S. Ricci, S. Hashemkhani, L. Boarino, D. Ielmini, C. Ricciardi, "In-materia reservoir computing with a fully memristive architecture based on self-organizing nanowire networks," Nature Mater. (2021). Doi: 10.1038/s41563-021-01099-9

[252] S. Bianchi, I. Muñoz-Martín, E. Covi, A. Bricalli, G. Piccoloni, A. Regev, G. Molas, J. F. Nodin, F. Andrieu, and D. Ielmini, "Combining accuracy and plasticity in convolutional neural networks based on resistive memory arrays for autonomous learning," IEEE J. Exploratory Solid-State Computational Devices and Circuits 7, 132-140 (2021). Doi: 10.1109/JXCDC.2021.3118061

[253] I. Muñoz-Martín, S. Bianchi, O. Melnic, A. G. Bonfanti, and D. Ielmini, "A drift-resilient hardware implementation of neural accelerators based on phase change memory devices," IEEE Trans. Electron Devices 68, 6076-6081 (2021). Doi: 10.1109/TED.2021.3118996

[254] M. Lanza, R. Waser, D. Ielmini, J. J. Yang, L. Goux, J. Sune, A. J. Kenyon, A. Mehonic, S. Spiga, V. Rana, S. Wiefels, S. Menzel, I. Valov, M. A. Villena, E. Miranda, X. Jing, F. Campabadal, M. Gonzalez, F. Aguirre, F. Palumbo, K. Zhu, J. B. Roldan, F. M. Puglisi, L. Larcher, T.-H. Hou, T. Prodromakis, Y. Yang, P. Huang, T. Wang, Y. Chai, K. L. Pey, N. Raghavan, S. Duenas, T. Wang, Q. Xia, S. Pazos, "Standards for the Characterization of Endurance in Resistive Switching Devices," ACS Nano (2021). DOI: 10.1021/acsnano.1c06980.

[255] P. Mannocci, G. Pedretti, E. Giannone, E. Melacarne, Z. Sun, and D. Ielmini, "A fully-analogue, universal primitive for linear algebra operations using resistive memories," IEEE Trans. Circuits and Systems I: Regular Papers 68, 4889-4899 (2021). DOI: 10.1109/TCSI.2021.3122278

[256] S. Wang, Z. Sun, Y. Liu, S. Bao, Y. Cai, D. Ielmini, and R. Huang," Optimization Schemes for In-Memory Linear Regression Circuit with Memristor Arrays," IEEE Trans. Circuits and Systems I: Regular Papers 68, 4900-4909 (2021). DOI: 10.1109/TCSI.2021.3122327

[257] P. Mannocci, A. Baroni, E. Melacarne, C. Zambelli, P. Olivo, E. Perez, C. Wenger and D. Ielmini, "In-memory principal component analysis by crosspoint array of resistive switching memory," IEEE Nanotechnology Magazine (2022).

[258] H. Lee, S. W. Cho, S. J. Kim, J. Lee, K. S. Kim, I. Kim, J.-K. Park, J. Y. Kwak, J. Kim, J. Park, Y.-J. Jeong, G. W. Hwang, K.-S. Lee, D. Ielmini, S. Lee, "Three-terminal Ovonic threshold switch (3T-OTS) with tunable threshold voltage for versatile artificial sensory neurons," Nano Letters (2022).

[259] M. Farronato, M. Melegari, S. Ricci, S. Hashemkhani, A. Bricalli, D. Ielmini, "Memtransistor devices based on MoS_2 multilayers with volatile switching due to Ag cation migration," Adv. Electronic Mater. (2022). DOI:10.1002/aelm.202101161

[260] N. Lepri, M. Baldo, P. Mannocci, A. Glukhov, V. Milo and D. Ielmini, "Modeling and compensation of IR drop in crosspoint accelerators of neural networks," IEEE Trans. Electron Devices (2022).

International Conference Proceedings

[261] M. Elena, D. Ielmini, A. Miotello and P. M. Ossi, "Structure and properties of sputter-deposited BN thin films," Elevated Temperature Coatings: Science and Technology II, TMS, N. B. Dahotre and J. M. Hampikian eds., 139-148 (1996). ISBN 0-87339-313-9

[262] G. Ghislotti, D. Ielmini, E. Riedo and M. Martinelli, "Picosecond time-resolved studies of defect-related recombination in high-resistivity CdTe, CdZnTe," Mat. Res. Soc. Symp. Proc., 510, 601-605 (1998). ISBN 1-55899-416-5

[263] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, "Impact ionization and stress-induced leakage current in thin gate oxides," Proc. ULIS 2000 Workshop, F. Balestra ed., 85-88 (2000). ISBN 2-9514840-0-3

[264] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, "Evidence for recombination at oxide defects and new SILC model," Proc. IRPS, 55-64 (2000). ISBN 0-7803-5860-0

[265] D. Ielmini, A. S. Spinelli, A. L. Lacaita and G. Ghidini, "Role of interface and bulk defect-states in the low-voltage leakage conduction of ultrathin oxides," Proc. Eur. Solid-State Device Res. Conf. 2000, Frontier Group, W. A. Lane et al. eds., 312-315 (2000). ISBN 2-86332-248-6

[266] D. Ielmini, A. S. Spinelli, A. L. Lacaita, D. J. DiMaria and G. Ghidini, "Experimental and numerical analysis of the quantum yield," IEDM Tech. Dig. 331-334 (2000). ISBN 0-7803-6438-4

[267] A. Modelli, F. Gilardoni, D. Ielmini and A. S. Spinelli "A new conduction mechanism for the anomalous bits in thin oxides Flash EEPROMs," Proc. IRPS, 61-66 (2001). ISBN 0-7803-6587-9

[268] D. Ielmini, A. S. Spinelli, A. L. Lacaita, L. Confalonieri and A. Visconti, "New technique for fast characterization of SILC distribution in Flash arrays," Proc. IRPS, 73-80 (2001). ISBN 0-7803-6587-9

[269] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, "Statistical modeling of reliability and scaling projections for Flash memories," IEDM Tech. Dig. 703-706 (2001). ISBN 0-7803-7050-3

[270] D. Ielmini, A. S. Spinelli, A. L. Lacaita, R. Leone and A. Visconti, “Localization of SILC in Flash memories after program/erase cycling,” Proc. IRPS, 1-6 (2002). ISBN 0-7803-7352-9
[271] D. Ielmini, A. S. Spinelli, A. Lacaita, M. Gubello and M. J. van Duuren, “Monitoring Flash EEPROM reliability by equivalent cell analysis,” Proc. Eur. Solid-State Device Res. Conf. 2002, University of Bologna, G. Baccarani et al. eds., 359-362 (2002). ISBN 88-900847-8-2
[272] D. Ielmini, A. S. Spinelli, A. L. Lacaita and M. J. van Duuren, “Correlated defect generation in thin oxides and its impact on Flash reliability,” IEDM Tech. Dig. 143-146 (2002). ISBN 0-7803-7462-2
[273] A. Chimenton, A. S. Spinelli, D. Ielmini, A. L. Lacaita, A. Visconti and P. Olivo, “Drain-accelerated degradation of tunnel oxides in Flash memories,” IEDM Tech. Dig. 167-170 (2002). ISBN 0-7803-7462-2
[274] A. S. Spinelli, D. Ielmini, A. L. Lacaita, A. Sebastiani and G. Ghidini, “Analysis of quantum yield in n-channel MOSFETs,” Proc. IRPS, 412-416 (2003). ISBN 0-7803-7649-8
[275] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, C. Previtali and C. Gerardi, “Study of data retention for nanocrystal Flash memories,” Proc. IRPS, 506-512 (2003). ISBN 0-7803-7649-8
[276] D. Ielmini, A. Ghetti, S. Beltrami, A. S. Spinelli, A. L. Lacaita and A. Visconti, “Experimental and Monte Carlo analysis of drain-avalanche hot-hole injection for reliability optimization in Flash memories,” IEDM Tech. Dig., 157-160 (2003). ISBN 0-7803-7872-5
[277] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, C. Gerardi, L. Perniola, B. De Salvo and S. Lombardo, “Program/erase dynamics and channel conduction in nanocrystal memories,” IEDM Tech. Dig., 549-552 (2003). ISBN 0-7803-7872-5
[278] B. De Salvo, C. Gerardi, S. Lombardo, T. Baron, L. Perniola, D. Mariolle, P. Mur, A. Toffoli, M. Gely, M. N. Semeria, S. Deleonibus, G. Ammendola, V. Ancarani, M. Melanotte, R. Bez, L. Baldi, D. Corso, I. Crupi, R. A. Puglisi, G. Nicotra, E. Rimini, F. Mazen, G. Ghibaudo, G. Pananakakis, C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, Y. M. Wan, K. van der Jeugd, “How far will Silicon nanocrystals push the scaling limits of NVMs technologies?,” IEDM Tech. Dig., 597-600 (2003). ISBN 0-7803-7872-5
[279] A. Itri, D. Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer and R. Bez, “Analysis of phase-transformation dynamics and estimation of amorphous-chalcogenide fraction in phase-change memories,” Proc. IRPS, 209-215 (2004). ISBN 0-7803-8315-X
[280] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, C. Gerardi and S. Lombardo, “Statistical analysis of nanocrystal memory reliability,” Proc. IRPS, 509-514 (2004). ISBN 0-7803-8315-X
[281] D. Ielmini, C. Monzio Compagnoni, A. S. Spinelli, A. L. Lacaita and C. Gerardi, “A new channel percolation model for Vt shift in discrete-trap memories,” Proc. IRPS, 515-521 (2004). ISBN 0-7803-8315-X
[282] A. L. Lacaita, A. Redaelli, D. Ielmini, M. Tosi, F. Pellizzer, A. Pirovano and R. Bez, “Programming and disturb characteristics in nonvolatile phase-change memories,” Proc. NVSM Workshop, 26-27 (2004).
[283] D. Ielmini, A. S. Spinelli, A. L. Lacaita, M. Robustelli, L. Chiavarone and A. Visconti, “High-energy oxide traps and anomalous soft-programming in Flash memories,” IEDM Tech. Dig., 493-496 (2004). ISBN 0-7803-8684-1
[284] A. L. Lacaita, A. Redaelli, D. Ielmini, F. Pellizzer, A. Pirovano, A. Benvenuti and R. Bez, “Electrothermal and phase-change dynamics in chalcogenide-based memories,” IEDM Tech. Dig., 911-914 (2004). ISBN 0-7803-8684-1
[285] C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita and R. Sotgiu, “Reliability assessment of discrete-trap memories for NOR applications,” Proc. IRPS, 240-245 (2005). ISBN 0-7803-8803-8
[286] D. Ielmini, D. Mantegazza, A. L. Lacaita, A. Pirovano and F. Pellizzer, “Effects of threshold switching and parasitic capacitance in the programming transient of chalcogenide phase-change memories,” Proc. International Conference on Memory Technology and Design, 195-198 (2005).
[287] A. Pirovano, F. Pellizzer, A. Redaelli, I. Tortorelli, E. Varesi, F. Ottogalli, M. Tosi, P. Besana, R. Cecchini, R. Piva, M. Magistretti, M. Scaravaggi, G. Mazzone, P. Petruzza, F. Bedeschi, T. Marangon, A. Modelli, D. Ielmini, A. L. Lacaita, and R. Bez, “uTrench phase-change memory cell engineering and optimization,” Proc. European Solid State Device Research Conference, 313-316 (2005).
[288] D. Ielmini, A. L. Lacaita, D. Mantegazza, F. Pellizzer and A. Pirovano, “Assessment of threshold switching dynamics in phase-change chalcogenide memories,” IEDM Tech. Dig., 897-900 (2005). ISBN 0-7803-9268-1
[289] R. Gusmeroli, A. S. Spinelli, C. Monzio Compagnoni, D. Ielmini, F. Morelli and A. L. Lacaita, “Program and SILC constraints on NC memories scaling: a Monte Carlo approach,” IEDM Tech. Dig., 1061-1064 (2005). ISBN 0-7803-9268-1
[290] A. Redaelli, D. Ielmini, A. L. Lacaita, F. Pellizzer, A. Pirovano and R. Bez, “Impact of crystallization statistics on data retention for phase change memories,” IEDM Tech. Dig., 761-764 (2005). ISBN 0-7803-9268-1
[291] D. Ielmini, A. S. Spinelli, A. L. Lacaita, L. Chiavarone and A. Visconti, “A new charge-trapping technique to extract SILC-trap time constants in SiO_2,” IEDM Tech. Dig., 551-554 (2005). ISBN 0-7803-9268-1
[292] R. Gusmeroli, A. S. Spinelli, C. Monzio Compagnoni, D. Ielmini, and A. L. Lacaita, “A Monte Carlo investigation of nanocrystal memory reliability,” 7th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSime, 1-5 (2006). ISBN I-4244-0276-X
[293] D. Mantegazza, D. Ielmini, A. Pirovano, B. Gleixner, A. L. Lacaita, E. Varesi, F. Pellizzer, and R. Bez, “Electrical characterization of anomalous cells in phase change memory arrays,” IEDM Tech. Dig., 53-56, 2006.
[294] D. Ielmini and Y. Zhang, “Physics-based analytical model of chalcogenide-based memories for array simulation,” IEDM Tech. Dig., 401-404, 2006. ISBN 1-4244-0438-X
[295] U. Russo, D. Ielmini and A. L. Lacaita, “A physics-based crystallization model for retention in phase-change memories,” Proc. IRPS, 547-553 (2007). ISBN 1-4244-0918-7
[296] D. Mantegazza, D. Ielmini, A. Pirovano, A. L. Lacaita, E. Varesi, F. Pellizzer and R. Bez, “Effects of the crystallization statistics on programming distributions in phase-change memory arrays,” International Conference on Memory Technology and Design, 43-46, 2007.
[297] U. Russo, A. Redaelli, D. Ielmini and A. L. Lacaita, “Geometry and material optimization for programming current scaling in phase change memory,” International Conference on Memory Technology and Design, 55-58, 2007.
[298] D. Mantegazza, D. Ielmini, E. Varesi, A. Pirovano and A. L. Lacaita, “Statistical analysis and modeling of programming and retention in PCM arrays,” IEDM Tech. Dig., 311-314, 2007.
[299] D. Ielmini, S. Lavizzari, D. Sharma and A. L. Lacaita “Physical interpretation, modeling and impact on phase change memory (PCM) reliability of resistance drift due to chalcogenide structural relaxation,” IEDM Tech. Dig., 939-942, 2007.

[300] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, S. Spiga, C. Wiemer, M. Perego and M. Fanciulli, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," IEDM Tech. Dig., 775-778, 2007.
[301] D. Ielmini, D. Sharma, S. Lavizzari and A. L. Lacaita, "Physical mechanism and temperature acceleration of relaxation effects in phase-change memory cells," Proc. IRPS, 597-603 (2008).
[302] S. Lavizzari, D. Ielmini, D. Sharma and A. L. Lacaita, "Structural relaxation in chalcogenide-based phase change memories (PCMs): from defect-annihilation kinetic to device-reliability prediction," E*PCOS, Prague, Czech Republic, Sept. 7-9, 2008.
[303] S. Lavizzari, D. Ielmini, D. Sharma and A. L. Lacaita, "Transient effects of delay, switching and recovery in phase change memory (PCM) devices," IEDM Tech. Dig., 215-218 (2008).
[304] C. Cagli, D. Ielmini, F. Nardi and A. L. Lacaita, "Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction," IEDM Tech. Dig., 301-304 (2008).
[305] D. Ielmini, M. Manigrasso, F. Gattel and G. Valentini, "A unified model for permanent and recoverable NBTI based on hole trapping and structure relaxation," Proc. IRPS, 26-32 (2009). ISBN: 978-1-4244-2889-2
[306] M. Boniardi, D. Ielmini, S. Lavizzari, A. L. Lacaita, A. Redaelli and A. Pirovano, "Statistical and scaling behavior of structural relaxation effects in phase change memory (PCM) devices," Proc. IRPS, 122-127 (2009). ISBN: 978-1-4244-2889-2
[307] A. Demolliens, Ch. Muller, and D. Deleruyelle, S. Spiga, E. Cianci, and M. Fanciulli, F. Nardi, C. Cagli, and D. Ielmini "Reliability of NiO-based resistive switching memory (ReRAM) elements with pillar W bottom electrode," International Memory Workshop 25-27 (2009).
[308] D. Fugazza, D. Ielmini, S. Lavizzari and A. L. Lacaita, "Distributed-Poole-Frenkel modeling of anomalous resistance scaling and fluctuations in phase-change memory (PCM) devices," IEDM Tech. Dig. 723-726 (2009).
[309] D. Ielmini, F. Nardi, A. Vigani, E. Cianci and S. Spiga," Read-disturb limited reliability of multilevel NiO-based resistive-switching memory," IEEE Semiconductor Interface Specialist Conference (SISC), Arlington, VA, Dec. 3-5, 2009.
[310] D. Ielmini, F. Nardi, C. Cagli and A. L. Lacaita, "Size-dependent temperature instability in NiO–based resistive switching memory," Mater. Res. Soc. Symp. Proc. 1250-G05-03, (2010).
[311] D. Fugazza, D. Ielmini, S. Lavizzari and A. L. Lacaita, "Random telegraph signal noise in phase change memory devices," IEEE IRPS 743-749 (2010).
[312] D. Ielmini, F. Nardi, C. Cagli and A. L. Lacaita, "Trade-off between data retention and reset in NiO RRAMs," IEEE IRPS 620-626 (2010).
[313] A. Calderoni, M. Ferro, D. Ventrice, D. Ielmini and P. Fantini, "Reset current distributions in Phase Change Memories," IEEE IRPS 738-742 (2010).
[314] M. Boniardi, D. Ielmini, A. L. Lacaita, A. Redaelli, A. Pirovano, I. Tortorelli, M. Allegra, "Impact of Material Composition on the write performance of Phase-Change Memory Devices, 2010 IEEE International Memory Workshop (IMW) 25-28 (2010).
[315] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, D. J. Wouters, "Sub-10 μA reset in NiO-based resistive switching memory (RRAM) cells," 2010 IEEE International Memory Workshop (IMW) 66-69 (2010).
[316] D. Ielmini, C. Cagli, F. Nardi and A. L. Lacaita, "Resistance-dependent switching in NiO-based filamentary RRAM devices," ISIF 211-212 (2010).
[317] G. Ferrari, A. Ghetti, D. Ielmini, A. Redaelli and A. Pirovano, "Multiphysics modeling of PCM devices for scaling investigation," SISPAD 265-268 (2010).
[318] D. Fugazza, D. Ielmini, G. Montemurro, and A. L. Lacaita, "Temperature- and time-dependent conduction controlled by activation energy in PCM," IEDM Tech. Dig. 652-655 (2010).
[319] D. Ielmini, F. Nardi, C. Cagli, "Universal switching and noise characteristics of nanofilaments in metal-oxide RRAMs," IEEE Semiconductor Interface Specialist Conference (SISC), San Diego, CA, Dec. 2-4, 2010.
[320] F. Nardi, C. Cagli, S. Spiga and D. Ielmini, "Reset current reduction and set-reset instabilities in unipolar NiO RRAM," International Memory Workshop 160-163 (2011).
[321] A. Calderoni, M. Ferro, D. Ventrice and P. Fantini and D. Ielmini, "Physical Modeling and Control of Switching Statistics in PCM Arrays," International Memory Workshop 138-141 (2011).
[322] S. Long, C. Cagli, D. Ielmini, M. Liu, J. Suñé, "Cell-based models for the switching statistics of RRAM," Nonvolatile Memory Technology Symposium (2011).
[323] C. Cagli, F. Nardi, B. Harteneck, Z. Tan, Y. Zhang and D. Ielmini, "Nanowire-based RRAM crossbar memory with metallic core–oxide shell nanostructure," Proc. European Solid-State Device Research Conference (ESSDERC), 103-106 (2011).
[324] F. Nardi, S. Balatti, S. Larentis and D. Ielmini, "Complementary switching in metal oxides: toward diode-less crossbar RRAMs," IEDM Tech. Dig. 709–712 (2011).
[325] N. Ciocchini, M. Cassinerio, D. Fugazza and D. Ielmini, "Modeling of threshold voltage drift in phase change memory (PCM) devices," Proc. International Memory Workshop (IMW) 151–154 (2012). DOI: 10.1109/IMW.2012.6213673
[326] S. Choi, S. Ambrogio, S. Balatti, F. Nardi and D. Ielmini, "Resistance drift model for conductive-bridge (CB) RAM by filament surface relaxation," Proc. International Memory Workshop (IMW) 123–126 (2012).
[327] S. Larentis, F. Nardi, S. Balatti, D. Gilmer and D. Ielmini, "Bipolar-switching model of RRAM by field- and temperature-activated ion migration," Proc. International Memory Workshop (IMW) 53–56 (2012).
[328] A. Calderoni, M. Ferro, E. Varesi, M. Rizzi, D. Ielmini and P. Fantini, "Investigation of Over-Reset programming in Phase Change Memory," Proc. International Memory Workshop (IMW) 159–162 (2012).
[329] S. Choi, S. Balatti, F. Nardi and D. Ielmini, "Nanofilament relaxation model for size dependent resistance drift in electrochemical memories," Technical Digest of Frontiers in Electronic Materials, J. Heber, D. Schlom, Y. Tokura, R. Waser and M. Wuttig, (Eds.), Wiley-VCH, 216–217 (2012). ISBN 978-3-527-41191-7
[330] M. Cassinerio, N. Ciocchini and D. Ielmini, "Inverse time voltage relation of threshold switching in phase change materials," Technical Digest of Frontiers in Electronic Materials, J. Heber, D. Schlom, Y. Tokura, R. Waser and M. Wuttig, (Eds.), Wiley-VCH, 125–126 (2012). ISBN 978-3-527-41191-7
[331] N. Ciocchini, M. Cassinerio, D. Fugazza and D. Ielmini, "Threshold voltage drift in phase change memories: scaling and modeling," Mater. Res. Soc. Symp. Proc. Vol. 1431 (2012). DOI: 10.1557/opl.2012.1315

[332] F. Xiong, M.-H. Bae, Y. Dai, A. D. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini and E. Pop, "Nanowire Phase Change Memory with Carbon Nanotube Electrodes," IEEE Device Research Conference, 215–216 (2012). ISBN 978-1-4673-1164-9

[333] N. Ciocchini, M. Cassinerio, D. Fugazza, and D. Ielmini, "Non-Arrhenius pulse-induced crystallization in phase change memories," IEDM Tech. Dig. 729-732 (2012).

[334] M. Rizzi and D. Ielmini, "Energy landscape model of conduction and switching in phase change memories," IEDM Tech. Dig. 589-592 (2012). DOI: 10.1109/IEDM.2012.6479106

[335] S. Balatti, S. Ambrogio, D. C. Gilmer and D. Ielmini, "Variability and failure of set process in HfO_x RRAM," Proc. International Memory Workshop (IMW) 38-41 (2013). ISBN 978-1-4673-6167-5. DOI: 10.1109/IMW.2013.6582092

[336] S. Ambrogio, S. Balatti, A. Cubeta, A. Calderoni, N. Ramaswamy and D. Ielmini, "Understanding switching variability and random telegraph noise in resistive RAM," IEDM Tech. Dig. 782-785 (2013). ISBN 978-1-4799-2306-9

[337] N. Ciocchini, E. Palumbo, M. Borghi, P. Zuliani, R. Annunziata and D. Ielmini, "Unified reliability modeling of Ge-rich phase change memory for embedded applications," IEDM Tech. Dig. 581 (2013). ISBN 978-1-4799-2306-9

[338] M. Rizzi, N. Ciocchini, A. Montefiori, M. Ferro, P. Fantini, A. L. Lacaita, and D. Ielmini, "Intrinsic retention statistics in phase change memory (PCM) arrays," IEDM Tech. Dig. (2013). ISBN 978-1-4799-2306-9

[339] S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Voltage-dependent random telegraph noise (RTN) in HfO_x resistive RAM," IEEE IRPS MY.4.1 – MY.4.6 (2014). DOI: 10.1109/IRPS.2014.6861159

[340] N. Ciocchini and D. Ielmini, "Modeling of crystallization kinetics in phase change memories for set and read disturb regimes," IEEE IRPS 5E.1.1 – 5E.1.6 (2014). DOI: 10.1109/IRPS.2014.6860675

[341] M. Rizzi, N. Ciocchini, A. Montefiori, M. Ferro, P. Fantini, A. L. Lacaita, and D. Ielmini, "Reset-induced variability of retention characteristics in phase change memory (PCM)," IEEE IRPS 5E.4.1 – 5E.4.6 (2014). DOI: 10.1109/IRPS.2014.6860679

[342] S. Ambrogio, S. Balatti, D. C. Gilmer and D. Ielmini, "Analytical modelling and leakage optimization in complementary resistive switch (CRS) crossbar arrays," Proc. ESSDERC 242-245 (2014). DOI: 10.1109/ESSDERC.2014.6948805

[343] M. Rizzi, N. Ciocchini, D. Ielmini, A. Ghetti and P. Fantini, "Set/reset statistics and kinetics in phase change memory arrays," Proc. ESSDERC 234-237 (2014). DOI: 10.1109/ESSDERC.2014.6948803

[344] M. Rizzi, N. Ciocchini, S. Caravati, M. Bernasconi, P. Fantini, and D. Ielmini, "Statistics of set transition in phase change memory (PCM) arrays," IEDM Tech. Dig. 701-704 (2014).

[345] S. Balatti, S. Ambrogio, Z.-Q. Wang, A. Calderoni, N. Ramaswamy and D. Ielmini, "Pulsed cycling operation and endurance failure of metal-oxide resistive RAM," IEDM Tech. Dig. 359-362 (2014).

[346] S. Ambrogio, S. Balatti, V. McCaffrey, D. Wang and D. Ielmini, "Impact of low-frequency noise on read distributions of resistive switching memory (RRAM)," IEDM Tech. Dig. 363-366 (2014).

[347] S. Balatti, S. Ambrogio, Z.-Q. Wang, S. Sills, A. Calderoni, N. Ramaswamy, and D. Ielmini, 'Understanding pulsed-cycling variability and endurance in HfO_x RRAM,' IEEE IRPS 5B3.1-5B3.6 (2015). DOI: 10.1109/IRPS.2015.7112744

[348] S. Ambrogio, S. Balatti, Z.-Q. Wang, Y.-S. Chen, H.-Y. Lee, F. Chen, and D. Ielmini, 'Data retention statistics and modelling in HfO_2 resistive switching memories,' IEEE IRPS MY.7.1-MY.7.6 (2015). DOI: 10.1109/IRPS.2015.7112810

[349] N. Ciocchini, M. Laudato, A. Leone, P. Fantini, A. L. Lacaita and D. Ielmini, "Universal thermoelectric characteristic in phase change memories," IEEE – International Memory Workshop (IMW), 1-4 (2015). DOI: 10.1109/IMW.2015.7150311

[350] Z.-Q. Wang, S. Ambrogio, S. Balatti, S. Sills, A. Calderoni, N. Ramaswamy and D. Ielmini, "Cycling-induced degradation of metal-oxide resistive switching memory (RRAM)," IEDM Tech. Dig. 173-176 (2015). DOI: 10.1109/IEDM.2015.7409649

[351] S. Ambrogio, S. Balatti, V. Milo, R. Carboni, Z. Wang, A. Calderoni, N. Ramaswamy, D. Ielmini, "Novel RRAM-enabled 1T1R synapse capable of low-power STDP via burst-mode communication and real-time unsupervised machine learning," Symp. VLSI Tech. Dig. (2016). DOI: 10.1109/VLSIT.2016.7573432

[352] N. Ciocchini, M. Laudato, A. L. Lacaita, D. Ielmini, M. Boniardi, E. Varesi, P. Fantini, "Bipolar-switching operated phase change memory (PCM) for improved high-temperature reliability," Proc. ESSDERC (2016). DOI: 10.1109/ESSDERC.2016.7599665

[353] A. Bricalli, E. Ambrosi, M. Laudato, M. Maestro, R. Rodriguez, and D. Ielmini, "SiO_x-based resistive switching memory (RRAM) for crossbar storage/select elements with high on/off ratio," IEDM Tech. Dig. 87 (2016).

[354] V. Milo, G. Pedretti, R. Carboni, A. Calderoni, N. Ramaswamy, S. Ambrogio, and D. Ielmini, "Demonstration of hybrid CMOS/RRAM neural networks with spike time/rate-dependent plasticity," IEDM Tech. Dig. 440 (2016). DOI: 10.1109/IEDM.2016.7838435

[355] R. Carboni, S. Ambrogio, W. Chen, M. Siddik, J. Harms, A. Lyle, W. Kula, G. Sandhu, and D. Ielmini, "Understanding cycling endurance in perpendicular spin-transfer torque (p-STT) magnetic memory," IEDM Tech. Dig. 572 (2016).

[356] G. Pedretti, V. Milo, R. Carboni, S. Bianchi, S. Ambrogio, and D. Ielmini, "Stochastic training and impact of noise in memristive neuromorphic hardware," Memrisys 2017, April 2-5, 2017, Athens, GR.

[357] G. Pedretti, S. Bianchi, V. Milo, A. Calderoni, N. Ramaswamy, and D. Ielmini, "Modeling-based design of brain-inspired spiking neural networks with RRAM learning synapses," IEDM Tech. Dig. 653-656 (2017). DOI: 10.1109/IEDM.2017.8268467

[358] V. Milo, E. Chicca, and D. Ielmini, "Brain-inspired recurrent neural network with plastic RRAM synapses," 2018 IEEE International Symposium Circuits and Systems (ISCAS), Firenze, Italy, May 4-7, 2018. Doi: 10.1109/ISCAS.2018.8351523

[359] W. Wang, A. Bricalli, M. Laudato, E. Ambrosi, E. Covi, and D. Ielmini, "Physics-based modeling of volatile resistive switching memory (RRAM) for crosspoint selector and neuromorphic computing," IEDM Tech. Dig. 932 (2018).

[360] O. Melnic, M. Borghi, E. Palumbo, P. Zuliani, R. Annunziata, D. Ielmini, "Monte Carlo model of resistance evolution in embedded PCM with Ge-rich GST," Symp. VLSI Tech. Dig. (2019).

[361] S. Bianchi, I. Muñoz-Martin, G. Pedretti, O. Melnic, S. Ambrogio and D. Ielmini, "Energy-efficient continual learning in hybrid supervised-unsupervised neural networks with PCM synapses," Symp. VLSI Tech. Dig. (2019).

[362] R. Carboni, E. Vernocchi, M. Siddik, J. Harms, A. Lyle, G. Sandhu and D. Ielmini, "A compact model of stochastic switching in STT magnetic RAM for memory and computing," 15th IEEE / ACM International Symposium on Nanoscale Architectures (NANOARCH), 17-19 July, 2019, Qingdao, China.

[363] V. Milo, C. Zambelli, P. Olivo, E. Pérez, O. G. Ossorio, Ch. Wenger and D. Ielmini, "Low-Energy Inference Machine with Multilevel HfO_2 RRAM Arrays," ESSDERC (2019).

[364] N. Polino, M. Laudato, E. Ambrosi, A. Bricalli and D. Ielmini, “Joule Heating in SiO_x RRAM Device Studied by an Integrated Micro-Thermal Stage,” ESSDERC 126-129 (2019).

[365] Z. Sun, G. Pedretti and D. Ielmini, “Fast solution of linear systems with analog resistive switching memory (RRAM),” 2019 International Conference on Rebooting Computing (ICRC) 2019. Doi: 10.1109/ICRC.2019.8914709

[366] E. Covi, Y.-H. Lin, W. Wang, T. Stecconi, A. Bricalli, E. Ambrosi, G. Pedretti, T.-Y. Tseng, and D. Ielmini, “A Volatile RRAM Synapse for Neuromorphic Computing,” ICECS (2019). DOI: 10.1109/ICECS46596.2019.8965044

[367] W. Wang, E. Covi, Y.-H. Lin, E. Ambrosi, and D. Ielmini, “Modeling of switching speed and retention time in volatile resistive switching memory by ionic drift and diffusion,” IEDM Tech. Dig. 763-766 (2019). Doi: 10.1109/IEDM19573.2019.8993625

[368] W. Wang, G. Pedretti, V. Milo, R. Carboni, A. Calderoni, N. Ramaswamy, A. S. Spinelli and D. Ielmini, “Computing of Temporal Information among Spikes using ReRAM Synapse,” Faraday Discussions 213, 453-469 (2019). DOI: 10.1039/c8fd00097b

[369] A. I. Berg, S. Brivio, S. Brown, G. Burr, S. Deswal, J. Deuermeier, E. Gale, H. Hwang, D. Ielmini, G. Indiveri, A. J. Kenyon, A. Kiazadeh, I. Köymen, M. Kozicki, Y. Li, D. Mannion, T. Prodromakis, C. Ricciardi, S. Siegel, M. Speckbacher, I. Valov, W. Wang, R. S. Williams, D. Wouters and Y. Yang, “Synaptic and neuromorphic functions: general discussion,” Faraday Discuss. 213, 553-578 (2019). DOI: 10.1039/C8FD90065E

[370] E. Ambrosi, P. Bartlett, A. I. Berg, S. Brivio, G. Burr, S. Deswal, J. Deuermeier, M. Haga, A. Kiazadeh, G. Kissling, M. Kozicki, C. Foroutan-Nejad, E. Gale, Y. Gonzalez-Velo, A. Goossens, L. Goux, T. Hasegawa, H. Hilgenkamp, R. Huang, S. Ibrahim, D. Ielmini, A. J. Kenyon, V. Kolosov, Y. Li, S. Majumdar, G. Milano, T. Prodromakis, N. Raeishosseini, V. Rana, C. Ricciardi, M. Santamaria, A. Shluger, I. Valov, R. Waser, R. S. Williams, D. Wouters, Y. Yang and A. Zaffora, “Electrochemical metallization ReRAMs (ECM) - Experiments and modelling: general discussion,” Faraday Discuss. 213, 115-150 (2019). DOI: 10.1039/C8FD90059K

[371] M. Aono, C. Baeumer, P. Bartlett, S. Brivio, G. Burr, M. Burriel, E. Carlos, S. Deswal, J. Deuermeier, R. Dittmann, H. Du, E. Gale, S. Hambsch, H. Hilgenkamp, D. Ielmini, A. J. Kenyon, A. Kiazadeh, A. Kindsmüller, G. Kissling, I. Köymen, S. Menzel, D. P. Asesio, T. Prodromakis, M. Santamaria, A. Shluger, D. Thompson, I. Valov, W. Wang, R. Waser, R. S. Williams, D. Wrana, D. Wouters, Y. Yang and A. Zaffora, “Valence change ReRAMs (VCM) - Experiments and modelling: general discussion,” Faraday Discuss. 213, 259-286 (2019). DOI: 10.1039/C8FD90057D

[372] P. Bartlett, A. I. Berg, M. Bernasconi, S. Brown, G. Burr, C. Foroutan-Nejad, E. Gale, R. Huang, D. Ielmini, G. Kissling, V. Kolosov, M. Kozicki, H. Nakamura, K. Rushchanskii, M. Salinga, A. Shluger, D. Thompson, I. Valov, W. Wang, R. Waser and R. S. Williams, “Phase-change memories (PCM) – Experiments and modelling: general discussion,” Faraday Discuss. 213, 393-420 (2019). DOI: 10.1039/C8FD90064G

[373] Z. Sun, G. Pedretti, E. Ambrosi, A. Bricalli and D. Ielmini, “In-memory PageRank using a Crosspoint Array of Resistive Switching Memory (RRAM) devices,” Proceedings - 2020 IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2020 26-30 (2020). Doi: 10.1109/AICAS48895.2020.9073964

[374] G. Pedretti, V. Milo, S. Hashemkhani, P. Mannocci, O. Melnic, E. Chicca, and D. Ielmini, “A spiking recurrent neural network with phase change memory synapses for decision making,” 2020 IEEE International Symposium Circuits and Systems (ISCAS), Seville, Spain, May 17-20, 2020. DOI: 10.1109/ISCAS45731.2020.9180513

[375] I. Muńoz-Martín, S. Bianchi, S. Hashemkhani, G. Pedretti and D. Ielmini, “Hardware Implementation of PCM-Based Neurons with self-Regulating Threshold for Homeostatic Scaling in Unsupervised Learning,” 2020 IEEE International Symposium Circuits and Systems (ISCAS), Seville, Spain, May 17-20, 2020. DOI: 10.1109/ISCAS45731.2020.9181033

[376] S. Bianchi, I. Muńoz-Martín, S. Hashemkhani, G. Pedretti and D. Ielmini, “A bio-Inspired Recurrent Neural Network with self-Adaptive Neurons and PCM Synapses for Solving Reinforcement Learning Tasks,” 2020 IEEE International Symposium Circuits and Systems (ISCAS), Seville, Spain, May 17-20, 2020.

[377] I. Muñoz-Martin, S. Bianchi, E. Covi, G. Piccolboni, A. Bricalli, A. Regev, J. F. Nodin, E. Nowak, G. Molas and D. Ielmini, “A SiOx RRAM-based hardware with spike frequency adaptation for power-saving continual learning in convolutional neural networks,” Symp. VLSI Tech. Dig. (2020). 10.1109/VLSITechnology18217.2020.9265072

[378] M. Baldo, O. Melnic, M. Scuderi, G. Nicotra, M. Borghi, E. Petroni, A. Motta, P. Zuliani, A. Redaelli and D. Ielmini, “Modeling of virgin state and forming operation in embedded phase change memory (PCM),” IEDM Tech. Dig. 267-270 (2020). DOI: 10.1109/IEDM13553.2020.9372089

[379] V. Milo, F. Anzalone, C. Zambelli, E. Pérez, M. Mahadevaiah, O. Ossorio, P. Olivo, C. Wenger, and D. Ielmini, “Optimized programming algorithms for multilevel RRAM in hardware neural networks,” IRPS (2021). DOI: 10.1109/IRPS46558.2021.9405119

[380] M. Baldo and D. Ielmini, “Modeling of oxide-based ECRAM programming by drift-diffusion ion transport,” International Memory Workshop (2021).

[381] A. Redaelli, A. Gandolfo, G. Samanni, E. Gomiero, E. Petroni, L. Scotti, A. Lippiello, P. Mattavelli, J. Jasse, D. Codegoni, A. Serafini, R. Ranica, C. Boccaccio, J. Sandrini, R. Berthelon, JC. Grenier, O. Weber, D. Turgis, A. Valery, S. Del Medico, V. Caubet, JP. Reynard, D. Dutartre, L. Favennec, A. Conte, F. Disegni, M. De Tomasi, A. Ventre, M. Baldo, D. Ielmini, A. Maurelli, P. Ferreira, F. Arnaud, F. Piazza, P. Cappelletti, R. Annunziata, R. Gonella, “Improving Ge-rich GST ePCM reliability through BEOL engineering,” ESSDERC (2021).

[382] A. Baroni, C. Zambelli, P. Olivo, E. Perez, C. Wenger, and D. Ielmini, ”Tackling the Low Conductance State Drift through Incremental Reset and Verify in RRAM arrays,” IIRW (2021).

[383] N. Lepri, A. Glukhov and D. Ielmini, “Mitigating read-program variation and IR drop by circuit architecture in RRAM-based neural network accelerators,” IRPS (2022).

[384] A. Glukhov, V. Milo, A. Baroni, N. Lepri, C. Zambelli, P. Olivo, E. Perez, C. Wenger and D. Ielmini, ”Statistical model of program/verify algorithms in resistive switching memories for in-memory neural network accelerators,” IRPS (2022).

Patents

[385] A. Visconti, M. Bonanomi, D. Ielmini and A. S. Spinelli, “Method for programming/erasing a non volatile memory cell device, in particular for flash type memories,” European Patent EP 1 833 058 A1, United States Patent Application US 2007/0211534 A1

[386] F. Pellizzer, D. Ielmini and A. Pirovano, “Reversing a potential polarity for reading phase change cells to shorten a recovery delay after programming”, United States Patent Application US 2011/0141799 A1
[387] M. Boniardi, A. Redaelli, F. Pellizzer, D. Ielmini and A. Pirovano, “MODIFIED RESET STATE FOR ENHANCED READ MARGIN OF PHASE CHANGE MEMORY” WO/2011/074021.
[388] D. Ielmini, S. Balatti, S. Ambrogio, and Z. Wang, ‘Electronic neuromorphic system, synaptic circuit with resistive switching memory and method of performing spike-timing dependent plasticity,’ US 10,650,308 B2.
[389] D. Ielmini, S. Balatti, and S. Ambrogio, ‘Random number generation from multiple memory states,’ WO 2017/153875 A1, US Patent App. 16/077,514
[390] P. Fantini, D. Ielmini, N. Ciocchini, “Apparatuses and methods for accessing variable resistance memory device,” US Patent 9,990,990
[391] D. Ielmini, Z. Sun, G. Pedretti, “Mathematical problem solving circuit comprising resistive elements,’ WO 2019/064215.

Daniele Ielmini is a Full Professor at the Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy. He received the Laurea (cum laude) and Ph.D. from Politecnico di Milano in 1995 e 2000, respectively. He held visiting positions at Intel Corporation (2006), Stanford University (2006) and the University of Illinois at Urbana-Champaign (2010). His research interests include non-volatile memories, such as phase change memory (PCM), resistive switching memory (RRAM), and spin-transfer torque magnetic memory (STT-MRAM), and novel in-memory computing circuits. In 2016, he coedited the book 'Resistive switching – from fundamental redox-processes to device applications' for Wiley-VCH. He authored/coauthored 15 book chapters, more than 300 papers published in international journals and presented at international conferences, and 8 patents. His works received more than 12,000 citations, with an H-index of 62 (Scopus, October 2021). He has served in several Technical Subcommittees of international conferences, such as IEEE-IEDM (2008-2009, 2017-2018), IEEE-IRPS (2006-2008), IEEE-SISC (2008-2010), INFOS (2011-2021) and IEEE-ISCAS (2016-2021). He is Associate Editor of IEEE Trans. Nanotechnology and Semiconductor Science and Technology. He received the Intel Outstanding Researcher Award in 2013, the ERC Consolidator Grant in 2014, and the IEEE-EDS Paul Rappaport Award in 2015. He is a Fellow of the IEEE.