CURRICULUM VITAE

Surname and Name	**Bertulessi Luca**
E-mail address	**luca.bertulessi@polimi.it**
ORCID	**0000-0001-6167-6512**
Scopus Author ID	**57191611496**

EDUCATION

PhD Date: May 2016 – Feb 2020
University: Politecnico di Milano
Degree Awarded: PhD in Information Technology – Electronics (cum Laude)
Thesis Title: "Frequency Synthesizers based on PLLs for Cellular Radio Applications"

MS Date: 2013 – 2015
University: Politecnico di Milano
Degree Awarded: Master of Electronics Engineering – LM-29
Thesis Title: "Analisi e progetto di un oscillatore LC ad alta efficienza a 3.6 GHz in CMOS 65 nm per terminali GSM"

BEng Date: 2010 – 2013
University: Politecnico di Milano
Degree Awarded: Bachelor of Electronics Engineering – L-8

WORK EXPERIENCE AND INTERNSHIP

Full-time Fixed-term Senior Researcher / Assistant Professor
Jul 2022 - Now
University, Politecnico di Milano, DEIB, Milano, Italy
Design of CMOS digitally intensive integrated circuits for next communications standards

Full-time Fixed-term Junior Researcher
Oct 2020 – Jul 2022
University, Politecnico di Milano, DEIB, Milano, Italy
Design of low-jitter digitally-intensive PLL (DPLL) in scaled CMOS technology for radar and 5G applications.

Temporary research fellowships / Post-Doctoral Researcher
Nov 2019 - Oct 2020
University, Politecnico di Milano, DEIB, Milano, Italy
Design methodologies of digital phase-locked loops at millimeter-wave in CMOS

Summer Internship, Mixed signal design engineer
Jun 2018 - Nov 2018
Automotive R&D, Infineon Technologies AG, Villach, Austria
Design of a 28nm CMOS Frequency synthesizers for automotive radar systems

Temporary research fellowships
Nov 2015 - May 2016
University, Politecnico di Milano, DEIB, Milano, Italy
Design of a high efficiency oscillator for a digital frequency synthesizer
in 65nm CMOS technology for wireless applications.

TEACHING EXPERIENCE

Lecturer
Mar 2023 – May 2023 (36h)
CEFRIEL - Politecnico di Milano, Milano, Italy
"Master Universitario di II livello" in Integrated Circuit Design
Module 8 – EDA DIGITAL AND MIXED-SIGNAL CIRCUITS
Lectures, exams and responsibility for the course.
Course topics: digital synthesis flow using commercial EDA, IC assembling and sign-off, mixed-signed simulations.

Lecturer
Sep 2022 – Nov 2022 (36h)
CEFRIEL - Politecnico di Milano, Milano, Italy
"Master Universitario di II livello" in Integrated Circuit Design
Module 7 – MICROELECTRONIC TECHNOLOGIES
Lectures, exams and responsibility for the course.
Course topics: Microelectronic technologies, devices physical implementation, PDK, DRM, Device models, Reliability and failure mechanisms, Antenna Effect, Planarity, Latch-up, ESD.

Assistant Professor
Sep 2021 - Now
Politecnico di Milano, DEIB, Milano, Italy
085746 - INTRODUCTION TO ELECTRONICS (10 CFU)
Bachelor Engineering of Computing Systems
Lectures and responsibility for the course.
Course topics: MOSFET, Diodes, Logic circuits, Memory circuits, Operational Amplifier, Analog to Digital and Digital to Analog converter, Electronic systems.

Teaching assistant
Feb 2021 - Jun 2021
Politecnico di Milano, DEIB, Milano, Italy
095264 - DIGITAL INTEGRATED CIRCUIT DESIGN (10CFU) - A.A. 20/21 –
Prof. Bonfanti Andrea Giovanni
Tutorial classes on digital electronic circuits.

Experimental teaching assistant
Mar 2018 - Jun 2018
Politecnico di Milano, DEIB, Milano, Italy
095274 - RF CIRCUIT DESIGN (10CFU) – A.A. 17/18 - Prof. Levantino Salvatore
Experimental lectures: LNA design and simulations.

AWARDS

Grant Switch2Product 2021 – Project HAwK December 2021
MADE Competence Center Industria 4.0,
via Giovanni Durando 10, Milano
Grant S2P and start-up acceleration program.

IT Ph.D. Springer Award May 2020
Politecnico di Milano – Milan -Italy
Best results from the Politecnico di Milano IT PhD program – 2020

RESEARCH EXPERIENCE

PhD researcher, Post-Doc Researcher, Full-time Researcher Dec 2015 – Now
ARPLab, Politecnico di Milano, DEIB, Milano, Italy

- Participation in more than 8 projects resulting in a silicon fabrication, measurements and publications
- More than 5 different technology process for circuit integration used, from 65nm to 28nm.
- Coordination of research projects activities.
- Management of CAD laboratory and measurements laboratory.
- H-index: 9 (Scopus March 2023)
- Citations: 250 (Scopus March 2023)

PUBLICATIONS

International Peer-Reviewed Journals publication

F. Buccoleri, S. Dartizio, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, D. Cherniak, **L. Bertulessi**, A. Bevilacqua, C. Samori, A.L. Lacaita, S: Levantino, "*A 72-fs-Total-Integrated-Jitter Two-Core Fractional-N Digital PLL With Digital Period Averaging Calibration on Frequency Quadrupler and True-in-Phase Combiner,*" in IEEE Journal of Solid-State Circuits, vol. 58, no. 3, pp. 634-646, March 2023, doi: 10.1109/JSSC.2022.3228899.

S. Dartizio, F. Buccoleri, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, D. Cherniak, **L. Bertulessi**, A. Bevilacqua, C. Samori, A.L. Lacaita, S: Levantino, "*A Fractional-N Bang-Bang PLL Based on Type-II Gear Shifting and Adaptive Frequency Switching Achieving 68.6 fs-rms-Total-Integrated-Jitter and 1.56 μs-Locking-Time,*" in IEEE Journal of Solid-State Circuits, vol. 57, no. 12, pp. 3538-3551, Dec. 2022, doi: 10.1109/JSSC.2022.3206955.

G.Bè, A. Parisi, **L. Bertulessi,** L. Ricci, L. Scaletti, M. Mercandelli, A.L. Lacaita, Andrea, S. Levantino, C. Samori, A. Bonfanti, "*A 900-MS/s SAR-Based Time-Interleaved ADC With a Fully Programmable Interleaving Factor and On-Chip Scalable Background Calibrations*," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 9, pp. 3645-3649, Sept. 2022, doi: 10.1109/TCSII.2022.3182217.

M. Mercandelli, **L. Bertulessi**, C. Samori and S. Levantino, "*A Digital PLL With Multitap LMS-Based Bandwidth Control*," in IEEE Solid-State Circuits Letters, vol. 5, pp. 126-129, 2022, doi: 10.1109/LSSC.2022.3173425.

L. Bertulessi, D. Cherniak, M. Mercandelli, C. Samori, A. L. Lacaita and S. Levantino, *"Novel Feed-Forward Technique for Digital Bang-Bang PLL to Achieve Fast Lock and Low Phase Noise,"* in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 5, pp. 1858-1870, May 2022, doi: 10.1109/TCSI.2022.3146788

M. Mercandelli, A. Santiccioli, A. Parisi, **L. Bertulessi,** D. Cherniak, Andrea L. Lacaita, C. Samori, Carlo and S. Levantino."*A 12.5-GHz Fractional-N Type-I Sampling PLL Achieving 58-fs Integrated Jitter*," in IEEE Journal of Solid-State Circuits, vol. 57, no. 2, pp. 505-517, Feb. 2022, doi: 10.1109/JSSC.2021.3123827.

S. Dartizio, F. Tesolin, M. Mercandelli, A. Santiccioli, A. Shehata, S. Karman, **L. Bertulessi,** F. Buccoleri, L. Avallone, A. Parisi, A.L. Lacaita, M.P. Kennedy, C. Samori, S. Levantino, "*A 12.9-to-15.1-GHz Digital PLL Based on a Bang-Bang Phase Detector With Adaptively Optimized Noise Shaping*," in IEEE Journal of Solid-State Circuits, vol. 57, no. 6, pp. 1723-1735, June 2022, doi: 10.1109/JSSC.2021.3116860.

A. Parisi, F. Tesolin, M. Mercandelli, **L. Bertulessi** and A. L. Lacaita, "*Self-Biasing Dynamic Startup Circuit for Current-Biased Class-C Oscillators,*" in IEEE Microwave and Wireless Components Letters, vol. 31, no. 9, pp. 1075-1078, Sept. 2021, doi: 10.1109/LMWC.2021.3094418.

A. Santiccioli, M. Mercandelli, **L. Bertulessi**, A. Parisi, D. Cherniak, A.L. Lacaita, Andrea, C. Samori, S. Levantino, "*A 66-fs-rms Jitter 12.8-to-15.2-GHz Fractional-N Bang–Bang PLL With Digital Frequency-Error Recovery for Fast Locking,*" in IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3349-3361, Dec. 2020, doi: 10.1109/JSSC.2020.3019344.

D. Cherniak, M. Mercandelli, **L.Bertulessi,** F. Padovan, L. Grimaldi, A. Santiccioli, M. Aichner, C. Samori, S. Levantino,"*A 250-Mb/s Direct Phase Modulator With −42.4-dB EVM Based on a 14-GHz Digital PLL*," in IEEE Solid-State Circuits Letters, vol. 3, pp. 126-129, 2020, doi: 10.1109/LSSC.2020.3006519.

L. Bertulessi ; S. Karman ; D. Cherniak ; A. Garghetti ; C. Samori ; A.L. Lacaita; S. Levantino, "*A 30-GHz Digital Sub-Sampling Fractional-N PLL With -238.6-dB Jitter-Power Figure of Merit in 65-nm LP CMOS*," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3493-3502, Dec. 2019, doi: 10.1109/JSSC.2019.2940332.

M. Mercandelli, L. Grimaldi, **L. Bertulessi**, C. Samori, A. L. Lacaita and S. Levantino, "*A Background Calibration Technique to Control the Bandwidth of Digital PLLs,*" in IEEE Journal of Solid-State Circuits, vol. 53, no. 11, pp. 3243-3255, Nov. 2018, doi: 10.1109/JSSC.2018.2866454.

D. Cherniak, L. Grimaldi, **L. Bertulessi**, R. Nonis, C. Samori and S. Levantino, "*A 23-GHz Low-Phase-Noise Digital Bang–Bang PLL for Fast Triangular and Sawtooth Chirp Modulation*," in IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3565-3575, Dec. 2018, doi: 10.1109/JSSC.2018.2869097.

International Peer-Reviewed Conferences Proceedings

L. Scaletti, G. Bè, A. Parisi, **L. Bertulessi,** L.Ricci, M. Mercandelli, S. Levantino, C. Samori, A. Bonfanti, "*A 10.2-ENOB, 150-MS/s Redundant SAR ADC With a Quasi-Monotonic Switching Algorithm for Time-Interleaved Converters,*" 2022 20th IEEE Interregional NEWCAS Conference (NEWCAS), Quebec City, QC, Canada, 2022, pp. 20-24, doi: 10.1109/NEWCAS52662.2022.9842195.

L.Ricci, L. Scaletti, G. Bè, **L. Bertulessi,** S. Levantino, C. Samori, A. Bonfanti, "*Concurrent Effect of Redundancy and Switching Algorithms in SAR ADCs*," 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 2022, pp. 900-904, doi: 10.1109/ISCAS48785.2022.9937809.

F. Buccoleri, S. Dartizio, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, A. Bevilacqua, **L. Bertulessi**, D. Cherniak, C. Samori, A.L. Lacaita, S. Levantino, "*A 9GHz 72fs-Total-Integrated-Jitter Fractional-N Digital PLL with Calibrated Frequency Quadrupler*," 2022 IEEE Custom Integrated Circuits Conference (CICC), Newport Beach, CA, USA, 2022, pp. 1-2, doi: 10.1109/CICC53496.2022.9772796.

S. Dartizio, F. Buccoleri, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, D. Cherniak, **L. Bertulessi**, A. Bevilacqua, C. Samori, A.L. Lacaita, S. Levantino,"*A 68.6fsrms-total-integrated-jitter and 1.56μs-locking-time fractional-N bang-bang PLL based on type-II gear shifting and adaptive frequency switching*," 2022 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022, pp. 1-3, doi: 10.1109/ISSCC42614.2022.9731683.

M. Mercandelli, **L. Bertulessi,** C. Samori and S. Levantino, "*A 3.7-to-4.1GHz Narrowband Digital Bang-Bang PLL with a Multitaps LMS Algorithm to Automatically Control the Bandwidth Achieving 183fs Integrated Jitter*," 2021 IEEE Asian Solid-State Circuits Conference (A-SSCC), Busan, Korea, Republic of, 2021, pp. 1-3, doi: 10.1109/A-SSCC53895.2021.9634706.

C. Samori and **L. Bertulessi**, "*Digital PLLs: the modern timing reference for radar and communication systems,*" ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 2021, pp. 21-27, doi: 10.1109/ESSCIRC53450.2021.9567810.

G. Be, M. Mercandelli and **L. Bertulessi**, "*A Timing Skew Correction Technique in Time-Interleaved ADCs Based on a DeltaSigma Digital-to-Time Converter*," SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME, online, 2021, pp. 1-4.

L. Scaletti, A. Parisi and **L. Bertulessi,** "*Skew and Jitter Performance in CMOS Clock Phase Splitter Circuits,*" SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME, online, 2021, pp. 1-4.

L. Ricci, **L. Bertulessi** and A. Bonfanti, "*A low-noise high-speed comparator for a 12-bit 200-MSps SAR ADC in a 28-nm CMOS process*," SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME, online, 2021, pp. 1-4.

A. Santiccioli, M. Mercandelli, S. Dartizio, F. Tesolin, S. Karman, A. Shehata, **L. Bertulessi,** F. Buccoleri, L. Avallone, A. Parisi, A.L. Lacaita, M.P. Kennedy, C. Samori, S. Levantino, "*32.8 A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays*," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 456-458, doi: 10.1109/ISSCC42613.2021.9365972.

M. Mercandelli, A. Santiccioli, S. Dartizio, A. Shehata, F. Tesolin, S. Karman, **L. Bertulessi,** F. Buccoleri, L. Avallone, A. Parisi, A.L. Lacaita, M.P. Kennedy, C. Samori, S. Levantino, "*32.3 A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter*," 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2021, pp. 445-447, doi: 10.1109/ISSCC42613.2021.9365768.

A. Santiccioli, M. Mercandelli, **L. Bertulessi**, A. Parisi, D. Cherniak, A. L. Lacaita, C. Samori and S. Levantino, "*17.2 A 66fsrmsJitter 12.8-to-15.2GHz Fractional-N Bang-Bang PLL with Digital Frequency-Error Recovery for Fast Locking,*" 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 268-270, doi: 10.1109/ISSCC19947.2020.9063094.

L. Grimaldi, **L. Bertulessi,** S. Karman, D. Cherniak, A. Garghetti, C. Samori, A. L. Lacaita, S. Levantino, "*16.7 A 30GHz Digital Sub-Sampling Fractional-N PLL with 198fsrms Jitter in 65nm LP CMOS*," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 268-270, doi: 10.1109/ISSCC.2019.8662411.

L. Bertulessi, L. Grimaldi, D. Cherniak, C. Samori and S. Levantino, "*A low-phase-noise digital bang-bang PLL with fast lock over a wide lock range,*" 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2018, pp. 252-254, doi: 10.1109/ISSCC.2018.8310279.

L. Bertulessi, S. Levantino and C. Samori, "*Analysis of power efficiency in high-performance class-B oscillators*," 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Lisbon, Portugal, 2016, pp. 1-4, doi: 10.1109/PRIME.2016.7519525.

Books Chapter

L. Bertulessi, Chapter: "*Frequency Synthesizers Based on Fast-Locking Bang-Bang PLL for Cellular Applications*", Special Topics in Information Technology, Springer International Publishing, 2021.

PROFESSIONAL AFFILIATIONS

IEEE Member, 2020-present

IEEE Student Member, 2016-2020

Solid-State Circuits Society Member, 2016-present

PROFESSIONAL SERVICE

Volunteer Reviewer for:

- IEEE Transactions on Circuits and Systems I : Regular Papers
- IEEE Journal of Solid-State Circuits

Volunteer Guest Editor for:

- Special Issue: "Electron Devices and Solid-State Circuits", Electronics, MDPI

LANGUAGES

Italian
English

OTHER

Amateur Radio Licence HAREC Level A CEPT 61-02