Curriculum Vitae

Updated on 24 Feb 2023

Surname and name	Levantino Salvatore
E-mail address	salvatore.levantino@polimi.it

Working experience

Dates	From 2021 to date
Name and address of the Employer	CEFRIEL, Milan, Italy
Position held	Director of Master Engineering Degree on IC Design
Main activities/responsibilities	Managing and Teaching

Dates	From 2019 to date
Name and address of the Employer	Politecnico di Milano, Milan, Italy
Position held	Tenured full professor of Electronics
Main activities/responsibilities	Teaching and research

Dates	From 2010 to 2019
Name and address of the Employer	Politecnico di Milano, Milan, Italy
Position held	Tenured associate professor of Electronics Teaching
Main activities/responsibilities	and research

Dates	From 2005 to 2010
Name and address of the Employer	
Position held	Politecnico di Milano, Milan, Italy
Main activities/responsibilities	Assistant professor of Electronics
	Teaching and research

Dates	
Name and address of the	From 2003 to 2007
Employer Position held	CEFRIEL, Milan, Italy
Main activities/responsibilities	Consultant on integrated circuit design
	Project Manager

Dates	
Name and address of the Employer	From 2000 to 2002
Position held	Nokia Bell Laboratories, Murray Hill (NJ)
	Consultant on integrated circuit design

Main activities/responsibilities	Research

Education and Training

Date	January 2002
Institution which issued the degree	Politecnico di Milano
Type of Degree awarded	Ph.D. in Electronics Engineering and Communications with thesis on "Fast-Hop Frequency Synthesizers for Wireless Systems"

Date	July 1998
Institution which issued the degree	Politecnico di Milano
Type of Degree awarded	Five-Year "Laurea" Degree (equivalent to Master Degree level) in Electronics Engineering

1. Scientific Activity

Salvatore Levantino provided significant research contributions in the field of **low-noise frequency synthesis in silicon technologies**. He introduced new architectures of digital phase-locked loops (PLLs) which substantially improved the jitter-power compromise and allowed to reach a record energy efficiency when used as wideband linear direct-FM modulators.

He provided new theoretical results describing the behavior and performance of **digital PLLs** based on bang-bang phase detectors. He introduced the so called digital-to-time converter (DTC) and a means to calibrate it in background, which extended the application of bang-bang PLLs to fractional-N frequency synthesis, for the first time.

Besides, he explained the mechanisms of flicker-noise up-conversion in oscillators and proposed new topologies and strategies for **low-noise oscillator design**. He also developed a theory of phase noise in **digital frequency dividers**, which is now widely adopted in scientific literature, and analyzed phase noise generation in oscillator arrays. He introduced a new architecture of radio receiver, consisting in an **IF-sampling receiver** with inherent anti-aliasing filtering.

Since 2020, he is also active in the field of **high-speed high-resolution analog-to-digital converters based on time-interleaving** with emphasis on algorithms and methods to correct the time-interleaving impairments. Since 2019, he has started a group focused on the design of **power management units** for general purpose, consumers, and industrial applications, investigating methods and architectures to improve the power density while preserving power efficiency, such as the time-based control of inductive DC/DC converters and the switched-capacitor DC/DC converters.

Since 1999, he co-authored **166 publications** (163 of which indexed in Scopus database), achieving 3,226 citations (Scopus source), divided in the following categories:

- 1 international textbook on frequency synthesizers (indexed in Scopus).
- 6 book chapters on digital PLLs and RF transmitters (5 indexed in Scopus).
- 69 papers and letters in international peer-reviewed journals (all indexed in Scopus).
- 87 conference papers appeared in the proceedings of international peer-reviewed conferences (85 indexed in Scopus).
- 3 editorials in international peer-reviewed journals.

He is also co-author of **10 patents**:

- 4 US issued patents.
- 6 patent applications.

The full list of publications is attached to this document.

He has an **H-index of 31** (Scopus source).

2. Coordination of Research and Technology Transfer Groups and Projects

- In Politecnico di Milano, in 2007, S. Levantino started up a research line focusing on digital RF circuits and systems. Over the years, the research was developed in collaboration with companies and research centers such as **Intel Labs**, Hillsboro (Oregon), **Imec**, Leuven (Belgium), **Infineon Technologies**, Villach (Austria), **STMicroelectronics**, Agrate (Italy).
- In June 2019, S. Levantino was nominated by Politecnico di Milano member of the steering committee of the **Joint Research Center between Infineon Technologies and Politecnico di Milano**, which has the aim of developing joint research in the field of CMOS radars for autonomous vehicles and 5G communications.
- In March 2021, S. Levantino was nominated by Politecnico di Milano member of the scientific committee of the **Joint Research Center between STMicroelectronics and Politecnico di Milano**, as representative of the research line focused on power management in BCD processes.
- Since 2007 to date, S. Levantino has supervised **9 PhD students** in the capacity of formal advisor and co-supervised **7 other PhD students**. Today, he is supervising or co-supervising **9 PhD students** and **1 post-Doc researcher** in the field of RF circuits, data converters and switched-mode power supplies.
- S. Levantino has had the scientific responsibility (as **Principal Investigator**) of **2 research projects funded by EU and the Italian Government** and **12 funded private research projects**, ruled through partnership agreements with companies or research institutions which are leaders in the semiconductor and IC design field.
- S. Levantino participated to **7 research projects funded by EU or the Italian Government**, and to other research collaborations ruled through partnership agreements, contributing to the design of wireless transceivers and phase-locked loops in BiCMOS and pure CMOS processes.
- S. Levantino developed **4 US issued patents** and **8 patent applications**.
- **Consulting** activity with *Accent S.r.l* (company providing microelectronic design services) from 2004 to 2006, in the role of project leader for the design of mixed-mode ASICs.
- **Consulting** activity with *CEFRIEL* (consortium of Politecnico di Milano for technology transfer) from 2003 to 2007 in the role of project manager for the design of ASICs.

3. National and International Reputation

3.1 Participation to the Editorial Boards of International Journals

- Member of the Editorial Board of *IEEE Journal of Solid-State Circuits*, in the capacity of **Guest Editor**, for the July-2012 Special Issue on the *47th IEEE European Solid-State Circuits Conference (ESSCIRC)*.
- Member of the Editorial Board of *IEEE Journal of Solid-State Circuits*, in the capacity of **Guest Editor**, for the May-2016 Special Issue on the *2015 IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium*.
- Member of the Editorial Board of *IEEE Transactions on Circuits and Systems-I: Regular Papers*, from January 2014 to December 2015, in the role of **Associate Editor**.
- Participation in the Editorial Board of *IEEE Transactions on Circuits and Systems-II: Express Briefs*, from January 2012 to December 2013, in the role of **Associate Editor**.

3.2 Official positions in international universities and research centers:

- **Visiting Scholar and Consultant** at *Bell Laboratories*, Murray Hill (NJ, USA) during the period from August 2000 to June 2002, invited by Dr. Mihai Banu and working in the field of CMOS architectures for GSM receivers and multi-gigahertz low-phase-noise oscillators. Here follow the exact periods spent in international research centers:
    - *Bell Labs, Lucent Technologies*, Murray Hill, NJ (USA) from August 2000 to April 2001
    - *Bell Labs, Agere Systems*, Murray Hill, NJ (USA) from July 2001 to September 2001
    - *Bell Labs, Agere Systems*, Murray Hill, NJ (USA) from February 2002 to May 2002.

3.3 Memberships and awards:

- Co-recipient of the **Best Paper Award** at the *2018 IEEE International Symposium on Circuits and Systems (ISCAS)* for the paper: A. Garghetti, A. L. Lacaita, S. Levantino, "A Low-Power and Wide-Locking-Range Injection-Locked Frequency Divider by Three with Dual-Injection Divide-by-Two Technique".
- Elected as 2018-2019 **IEEE Distinguished Lecturer** for SSCS society.
- Co-recipient of the 2012-2013 **Best Associate Editor Award** of *IEEE Transactions on Circuits and Systems-II*.
- **Senior Member of IEEE** since 2016.
- Member of IEEE since 1999, member of *IEEE Solid-State Circuits Society* since 1999, member of *IEEE Circuits and Systems Society* since 2010.

3.4 Participation to International Conferences as invited speaker:

- **Keynote speaker** at IEEE VLSI-SoC2022 "Designing Phase-Locked Loops in Modern CMOS Technologies", Patras (Greece), October 3, 2022.
- **Invited speaker** "*Recent Advances in High-Performance Frequency Synthesizer Design*" at 2022 IEEE Custom Integrated Circuits Conference (CICC), on April 26, 2022.
- **Invited IEEE Distinguished Lecturer** "*Basics of Digital Phase Locked Loops*", sponsored by IEEE SSCS, University of Texas, Austin (TX), 18 April 2019.
- **Invited speaker** "*Digitally-Intensive Fast Frequency Modulators for FMCW Radars*" at 2019 IEEE Custom Integrated Circuits Conference (CICC), held in Austin (TX) on April 14-17, 2019.
- **Invited IEEE Distinguished Lecturer** "*Wideband Linear Phase/Frequency Modulators in CMOS*", sponsored by IEEE Solid-State Circuit Society, Tyndall National Institute, Cork (Ireland), 28 August 2018.
- **Invited tutorial speaker** "*Digital Phase Locked Loops*" at 2018 IEEE Custom Integrated Circuits Conference (CICC), held in San Diego (CA) on April 8-11, 2018.

- **Workshop organizer** "*High Performance Power Efficient Clock Generation for Internet of Things Applications*" at the 2017 IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium, held in Honolulu (HI) on June 4th, 2017
- **Invited speaker** "*Mostly-Digital Phase Locked Loops*" at CAS Workshop 2017, held in Pavia (Italy) on March 20th, 2017.
- **Invited tutorial speaker** "*Quick Start Guide of Digital PLL for Digital Designers*" at the 2017 Asia and South Pacific Design Automation Conference (ASP-DAC), held in Tokyo (Japan) on Jan. 16th, 2017**.**
- **Invited paper** "*Digital Phase Locked Loops*" at the 2016 IEEE European Solid-State Circuits Conference (ESSCIRC), held in Lausanne (Switzerland) on Sep. 14th, 2016.
- **Invited workshop speaker** "*Frequency Synthesizers based on Realigned Oscillators*" at the 2016 IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium, held in San Francisco (CA) on May 22nd, 2016.
- **Invited tutorial** "*Advanced Digital Phase-Locked Loops*" at the IEEE CASS 2014 Outreach Initiative on Advanced Topics in Microelectronic Engineering ATIME 2015/01, held in Limerick (Ireland) on June 8th, 2015.
- **Workshop organizer** "Highly-Efficient RF Frequency Generation in Nanometer CMOS Technologies" at the 2015 IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium, held in Phoenix (AZ) on May 2015.
- **Invited tutorial** "*The Basics of Digital PLLs*" at the IEEE CASS 2013 Outreach Initiative Workshop on Developing Inter-Disciplinary Education in Circuits and Systems Community, held in Milan (Italy) on March 6th, 2014.
- **Invited paper** "*Nonlinearity Cancellation in Digital PLLs*" at the 2013 IEEE Custom Integrated Circuits Conference (CICC) held in San Jose (CA) on Sep. 2013.
- **Invited tutorial** "*Advanced Digital Phase-Locked Loops*" at the 2013 IEEE Custom Integrated Circuits Conference (CICC), held in San Jose (CA) on Sep. 2013.
- **Invited workshop** "*Nonlinearity Mitigation in Digital PLLs for High-Performance Transmitter*s" at the 2013 IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium, held in Seattle (WA) on June 2013.

3.5 Participation to Committees of International Conferences:

- **Member of the Technical Program Committee** of *IEEE International Solid-State Circuits Conference (ISSCC)* from 2020 to 2023 (4 years).
- **Committee member** of the Student Research Preview (SRP) of *IEEE International Solid-State Circuits Conference (ISSCC)* from 2018 to 2019 (2 years).
- **Member of the Technical Program Committee** of *IEEE European Solid-State Circuits Conference (ESSCIRC)* from 2019 to 2022 (4 years).
- **Member of the Steering Committee** of *IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium* in the role of *Signs and Sessions Chair*, *Transactions Chair*, *European Liaison* from 2015 to 2017 (3 years).
- **Member of the Technical Program Committee** of *IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium* from 2012 to 2019 (8 years) and **Sub-Committee Chair** (Frequency Generation Circuits) from 2016 to 2019 (4 years).
- **Session Chair** at *IEEE European Solid-State Circuits Conference (ESSCIRC)* (2022), of *IEEE International Solid-State Circuits Conference (ISSCC)* (2020)*, IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium* (2012, 2014, 2018).

4. Teaching Activities

Nineteen years of teaching experience at **graduate** level in the School of Engineering at Politecnico di Milano:

- *Thirteen years* of formal responsibility of the graduate course of ***"RF Circuit Design"***, 10 ECTS, for the Master of Science's degree in Electronics Engineering at Politecnico di Milano, from 2010/2011 to date. Since 2014/2015, the course has been taught in English.
- *Six years* of formal responsibility of the graduate course of ***"Integrated Systems for Communications"***, 5 ECTS, for the Master of Science's degree in Electronics Engineering at Politecnico di Milano, from 2004/2005 to 2009/2010.

Eleven years of teaching experience at **undergraduate** level in the School of Engineering at Politecnico di Milano:

- *Five years* of formal responsibility of the undergraduate course of ***"Electronics Foundations"***, 10 ECTS, for the Bachelor's Degree in Computer Science Engineering at Politecnico di Milano, from academic year 2015/2016 to 2020/2021 (excluding 2016/2017).
- *Four years* as assistant professor of the undergraduate course of ***"Analog Electronics"***, 10 ECTS, for the Bachelor's Degree in Electronics Engineering at Politecnico di Milano, from 2002/2003 to 2005/2006 (40 hours of teaching per academic year).
- *Five years* as laboratory assistant of the course of ***"Electronics Foundations"***, 10 ECTS, for the Bachelor's Degree in Electronics Engineering at Politecnico di Milano, from 2001/2002 to 2005/2006 (12 hours of classes per academic year).

Full List of Publications

I. Books:

1. A. L. Lacaita, **S. Levantino**, C. Samori, *Integrated Frequency Synthesizers for Wireless Systems*, Cambridge University Press, Cambridge (UK), 2007, 240 pages. ISBN-13: 9780521863155. DOI 10.1017/CBO9780511541131

II. Book Chapters:

1. S.L.J. Gierkink, **S. Levantino**, R.C. Frye, V. Boccuzzi, "A low phase noise 5GHz Quadrature CMOS VCO using common mode inductive coupling," *Phase-Locking in High-Performance Systems: From Devices to Architectures* (edited by B. Razavi), 2003, pp. 310-313, ISSN 978-047054549-2. DOI 10.1109/9780470545492.ch35
2. **S. Levantino** and C. Samori, "Digital Fractional-N Frequency Synthesis", Chapter 5 in *Advances in Analog and RF IC Design for Wireless Communication Systems* (edited by G. Manganaro and D. Leenaerts) Elsevier, 2013, pp. 83-113, ISBN 9780123983268. DOI 10.1016/B978-0-12-398326-8.00005-4
3. **S. Levantino**, G. Marzin, C. Samori, "All-Digital Phase-Locked Loops for Linear Wideband Phase Modulation", Chapter 16 in *Wireless Transceiver Circuits: System Perspectives and Design Aspects* (edited by W. Rhee), CRC Press, 2015, pp. 427-444, ISBN 9781482234350.
4. **S. Levantino,** C. Samori, "Low Power RF Digital PLLs with Direct Carrier Modulation," Chapter 9 in IoT and *Low-Power Wireless: Circuits, Architectures, and Techniques* (edited by C. Siu), CRC Press, 2018, ISBN 9780815369714.
5. **S. Levantino** and C. Samori, "Bang-bang digital PLLs for wireless systems," Chapter 6 in *Phase-Locked Frequency Generation and Clocking: Architectures and circuits for modern wireless and wireline systems (Control, Robotics and Sensors)* (edited by W. Rhee), IET, June 2020, pp. 141-168, ISBN 978-1785618857.
6. D. Cherniak and **S. Levantino**. "Chirp Generators for Millimeter-Wave FMCW Radars," *SpringerBriefs in Applied Sciences and Technology*, 2020, pp. 33-47, ISSN 2191-530X.

III. Papers in International Peer-Reviewed Journals:

1. C. Samori, A. L. Lacaita, A. Zanchi, **S. Levantino**, G. Calì, "Phase Noise Degradation at High Oscillation Amplitude in LC-tuned VCO's", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 96-99, Jan. 2000. ISSN 0018-9200. DOI 10.1109/4.818924
2. A. Zanchi, C. Samori, **S. Levantino**, A. L. Lacaita, "A 2-V 2.5-GHz –104-dBc at 100 kHz fully integrated VCO with wide-band low-noise automatic amplitude control loop", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, pp. 611-619, Apr. 2001. ISSN 0018-9200. DOI 10.1109/4.913739
3. C. Samori, A. Zanchi, **S. Levantino**, A.L. Lacaita, "A Fully Integrated Low-Power Low-Noise 2.6 GHz Bipolar VCO for Wireless Applications", *IEEE Microwave and Wireless Components Letters*, vol. 11, no. 5, pp. 199-201, May 2001. ISSN 1531-1309. DOI 10.1109/7260.923027
4. A. Zanchi, C. Samori, A. L. Lacaita, **S. Levantino**, "Impact of AAC Design on Phase Noise Performance of VCOs", *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 48, no. 6, pp. 537-547, June 2001. ISSN 1057-7130. DOI 10.1109/82.943325
5. C. Samori, **S. Levantino**, A. L. Lacaita, "Integrated LC Oscillators for Frequency Synthesis in Wireless Applications", *IEEE Communications Magazine*, vol. 40, no. 5, pp. 166-171, May 2002. ISSN 0163-6804. DOI 10.1109/35.1000231
6. **S. Levantino**, C. Samori, A. Zanchi, A. L. Lacaita, "AM-to-PM Conversion in Varactor-Tuned Oscillators", *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 49, pp. 509-513, July 2002. ISSN 1057-7130. DOI 10.1109/TCSII.2002.804051
7. **S. Levantino**, C. Samori, S. Gierkink, A. Bonfanti, A.L. Lacaita, V. Boccuzzi, "Frequency Dependence on Bias Current in 5-GHz CMOS VCOs': Impact on Tuning and Flicker Noise Up-Conversion", *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1003-1011, Aug. 2002. ISSN 0018-9200. DOI 10.1109/JSSC.2002.800969
8. **S. Levantino**, C. Samori, M. Banu, J. Glas, V. Boccuzzi, "A CMOS GSM IF Sampling Circuit with Reduced In-Channel Aliasing", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 895-904, June 2003. ISSN 0018-9200. DOI 10.1109/JSSC.2003.811871

9. S. Gierkink, **S. Levantino**, R. Frye, C. Samori, V. Boccuzzi, "A Low-Phase-Noise 5-GHz CMOS Quadrature VCO using Superharmonic Coupling", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1148-1154, July 2003. ISSN 0018-9200. DOI 10.1109/JSSC.2003.813297
10. S. Pellerano, **S. Levantino**, C. Samori, A.L. Lacaita, "A 13.5-mW 5-GHz Frequency Synthesizer with Dynamic Logic Frequency Divider", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 378-38, Feb. 2004. ISSN 0018-9200. DOI 10.1109/JSSC.2003.821784
11. **S. Levantino**, L. Romanò, S. Pellerano, C. Samori, A.L. Lacaita, "Phase Noise in Digital Frequency Dividers", *IEEE Journal of Solid-State Circuits,* vol. 39, no. 5, pp. 775-784, May 2004. ISSN 0018-9200. DOI 10.1109/JSSC.2004.826338
12. **S. Levantino**, M. Milani, C. Samori, A. Lacaita, "Fast-Switching Analog PLL with Finite-Impulse Response," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 51, no. 9, pp. 1697-1701, Sept. 2004. ISSN 1549-8328. DOI 10.1109/TCSI.2004.834519
13. **S. Levantino**, A. Bonfanti, L. Romano', C. Samori, A. L. Lacaita, "Differentially-Tuned VCO with Reduced Tuning Sensitivity and Flicker Noise Up-Conversion," *Springer Analog Integrated Circuits and Signal Processing*, vol. 42, no. 1, pp. 21-29, January 2005. DOI 10.1023/B:ALOG.0000042324.94775.62
14. A. Bonfanti, **S. Levantino**, C. Samori, A. Lacaita, "A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 53, no.3, pp. 481-488, March 2006. ISSN 1549-8328. DOI 10.1109/TCSI.2005.858764
15. L. Romanò, **S. Levantino**, C. Samori, A. Lacaita, "Multiphase LC oscillators," *IEEE Transactions on Circuits and Systems – I: Regular Papers,* vol. 53, no.7, pp. 1579-1588, July 2006. ISSN 1549-8328. DOI 10.1109/TCSI.2006.876415
16. L. Romanò, A. Bonfanti, **S. Levantino**, C. Samori, A.L. Lacaita, "5-GHz Oscillator Array With Reduced Flicker Up-Conversion in 0.13-µm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 41, no.11, pp. 2457-2467, Nov. 2006. ISSN 0018-9200. DOI 10.1109/JSSC.2006.883315
17. P. Madoglio, M. Zanuso, **S. Levantino**, C. Samori, A.L. Lacaita, "Quantization Effects in All-Digital Phase-Locked Loops," *IEEE Transactions on Circuits and Systems-II*, vol. 54, no. 12, pp. 1120-1124, Dec. 2007. ISSN 1549-7747. DOI 10.1109/TCSII.2007.906171
18. L. Panseri, L. Romanò, **S. Levantino**, C. Samori, A.L. Lacaita, "Low-Power Signal Component Separator for a 64-QAM 802.11 LINC Transmitter," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1274-1286, May 2008. ISSN 0018-9200. DOI 10.1109/JSSC.2008.920321
19. M. Zanuso, D. Tasca, **S. Levantino**, A. Donadel, C. Samori, and A. L. Lacaita, "Noise Analysis and Minimization in Bang-Bang Digital PLL," *IEEE Transactions on Circuits and Systems - II: Express Briefs*, vol. 56, no. 11, pp. 835-839, Nov. 2009. DOI 10.1109/TCSII.2009.2032470
20. M. Zanuso, P. Madoglio, **S. Levantino**, C. Samori, A. L. Lacaita, "Time-to-Digital Converter for Frequency Synthesis based on a Digital Bang-Bang DLL*," IEEE Transactions Circuits Systems - I: Regular Papers,* vol. 57, no. 3, pp. 548–555, Mar. 2010. ISSN 1549-8328. DOI 10.1109/TCSI.2009.2023945
21. **S. Levantino**, M. Zanuso, P. Madoglio, D. Tasca, C. Samori, A. L. Lacaita, "AD-PLL for WiMAX with Digitally-Regulated TDC and Glitch Correction Logic," *EURASIP Journal on Embedded Systems*, vol. 2010, no. 175764 (12 November 2009), pp. 1-8, 2010. DOI 10.1155/2010/175764
22. **S. Levantino**, L. Collamati, C. Samori, A. L. Lacaita, "Folding of Phase Noise Spectra in Charge-Pump Phase-Locked Loops Induced by Frequency Division," *IEEE Transactions Circuits Systems - II: Express Briefs*, vol. 57, no. 9, pp. 671–675, Sep. 2010. DOI 10.1109/TCSII.2010.2056072
23. M. Zanuso, **S. Levantino**, C. Samori, and A. L. Lacaita, "A Wideband 3.6 GHz Digital ΔΣ Fractional-N PLL With Phase Interpolation Divider and Digital Spur Cancellation," *IEEE Journal Solid-State Circuits*, vol. 46, no. 3, pp. 627-638, Mar. 2011. ISSN 0018-9200. DOI 10.1109/JSSC.2010.2104270
24. D. Tasca, M. Zanuso, **S. Levantino**, C. Samori, A. L. Lacaita, "Low-Power Divider Retiming in a 3-4GHz Fractional-N PLL," *IEEE Transactions Circuits Systems - II: Express Briefs*, vol. 58, no. 4, pp. 200–204, Apr. 2011. ISSN 1549-7747. DOI 10.1109/TCSII.2011.2124510
25. D. Tasca, M. Zanuso, G. Marzin, **S. Levantino**, C. Samori, and A. L. Lacaita, "A 2.9-to-4.0GHz Fractional-N Digital PLL with Bang-Bang Phase Detector and 560fsrms Integrated Jitter at 4.5mW Power," *IEEE Journal Solid-State Circuits,* vol. 46, no. 12, pp. 2745–2758, Dec. 2011. ISSN 0018-9200. DOI 10.1109/JSSC.2011.2162917
26. P. Maffezzoni, **S. Levantino**, "Computing low-frequency noise in charge-pump phase-locked loops," *IET Electronics Letters*, vol. 47, no. 23, pp. 1270-1272, Nov. 2011. ISSN 0013-5194. DOI 10.1049/el.2011.2712

27. M. Zanuso, **S. Levantino**, C. Samori, A. L. Lacaita, "A Glitch-Corrector Circuit for Low-Spur ADPLLs," *Springer Analog Integrated Circuits and Signal Processing*, vol. 73, no. 1, pp. 201-208, Oct. 2012. DOI 10.1007/s10470-011-9809-0
28. P. Maffezzoni, **S. Levantino**, "Analysis of VCO Phase Noise in Charge-Pump Phase-Locked Loops," *IEEE Transactions Circuits Systems - I: Regular Papers*, vol. 59, no. 10, pp. 2165–2175, Oct. 2012. ISSN 1549-8328. DOI 10.1109/TCSI.2012.2185312
29. **S. Levantino**, P. Maffezzoni, "Computing the Perturbation-Projection-Vector of Oscillators via Frequency Domain Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 10, pp. 1499-1507, Oct. 2012. ISSN 0278-0070. DOI 10.1109/TCAD.2012.2194493
30. **S. Levantino**, P. Maffezzoni, F. Pepe, A. Bonfanti, C. Samori, A. L. Lacaita, "Efficient Calculation of the Impulse Sensitivity Function in Oscillators," *IEEE Transactions Circuits Systems - II: Express Briefs*, vol. 59, no. 10, pp. 628-632, Oct. 2012. ISSN 1549-7747. DOI 10.1109/TCSII.2012.2208679
31. P. Maffezzoni, **S. Levantino**, "Phase-Noise Analysis and Simulation of LC Oscillator-based Injection-Locked Frequency Dividers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 31, no.12, pp. 1925-1929, Dec. 2012. ISSN 0278-0070. DOI 10.1109/TCAD.2012.2205927
32. G. Marzin, **S. Levantino**, C. Samori, A. L. Lacaita, "A 20 Mb/s Phase Modulator Based on a 3.6GHz Digital PLL with -36dB EVM at 5mW Power," *IEEE Journal Solid-State Circuits*, vol. 47, no. 12, pp. 2974-2988, Dec. 2012. ISSN 0018-9200.DOI 10.1109/JSSC.2012.2217854
33. F. Pepe, A. Bonfanti, **S. Levantino**, C. Samori, A. L. Lacaita, "Analysis and Minimization of Flicker Noise Up-Conversion in Voltage-Biased Oscillators," *IEEE Trans. on Microwave Theory and Techniques*, vol. 61, no. 6, pp. 2382-2394, Jun. 2013. ISSN 0018-9480. DOI 10.1109/TMTT.2013.2259257
34. P. Maffezzoni, G. Marucci, **S. Levantino**, C. Samori, "Comparing techniques for spur reduction in digital bang-bang PLLs," Electronics Letters, vol. 49, pp. 527-529, Aug. 2013. ISSN 0013-5194. DOI 10.1049/el.2012.4402
35. F. Pepe, A. Bonfanti, **S. Levantino**, C. Samori, A.L. Lacaita, "Suppression of Flicker Noise Up-Conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz Band," *IEEE Journal of Solid-State Circuits*, 48, pp. 2375-2389, Oct. 2013. ISSN 0018-9200. DOI 10.1109/JSSC.2013.2273181
36. **S. Levantino**, G. Marzin, C. Samori, A.L. Lacaita, "A Wideband Fractional-N PLL With Suppressed Charge-Pump Noise and Automatic Loop Filter Calibration," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 2419-2429, Oct. 2013. ISSN 0018-9200. DOI 10.1109/JSSC.2013.2273836
37. G. Marucci, **S. Levantino**, P. Maffezzoni, C. Samori "Exploiting Stochastic Resonance to Enhance the Performance of Digital Bang-Bang PLLs," *IEEE Transactions on Circuits and Systems-II: Express Briefs,* vol. 60, pp. 632-636, Oct. 2013. ISSN 1549-7747. DOI 10.1109/TCSII.2013.2273732
38. G. Marucci, **S. Levantino**, P. Maffezzoni, C. Samori, "Analysis and Design of Low-Jitter Digital Bang-Bang Phase-Locked Loops," *IEEE Transactions on Circuits and Systems-I: Regular Papers,* vol. 61, pp. 26-36, Jan. 2014. ISSN 1549-8328. DOI 10.1109/TCSI.2013.2268514
39. **S. Levantino**, G. Marzin, C. Samori, "An Adaptive Pre-Distortion Technique to Mitigate the DTC Nonlinearity in Digital PLLs," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 1762-1772, Aug. 2014. ISSN 0018-9200. DOI 10.1109/JSSC.2014.2314436
40. P. Maffezzoni, **S. Levantino**, "Phase Noise of Pulse Injection-Locked Oscillators," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 61, pp. 2912-2919, Oct. 2014. ISSN 1549-8328. DOI 10.1109/TCSI.2014.2321200
41. **S. Levantino**, G. Marucci, G. Marzin, A. Fenaroli, C. Samori, A.L. Lacaita, "A 1.7-GHz Fractional-N Frequency Synthesizer based on a Multiplying Delay-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 2678-2691, Nov. 2015. ISSN 0018-9200. DOI 10.1109/JSSC.2015.2473667
42. A. Santiccioli, C. Samori, A. L. Lacaita, **S. Levantino**, "Power-jitter trade-off analysis in digital-to-time converters," in *IET Electronics Letters*, vol. 53, pp. 306-308, May 2017. ISSN 0013-5194. DOI 10.1049/el.2016.4577
43. D. Cherniak, C. Samori, R. Nonis, **S. Levantino**, "PLL-Based Wideband Frequency Modulator: Two-Point Injection Versus Pre-Emphasis Technique," *IEEE Trans. on Circuits and Systems-I*, vol. 65, pp. 914-924, March 2018. ISSN 1549-8328 DOI 10.1109/TCSI.2017.2763581
44. M. Leoncini, A. Bonfanti, **S. Levantino**, A. L. Lacaita, "Efficient Behavioral Simulation of Charge-Pump Phase-Locked Loops," *IEEE Trans. on Circuits and Systems-I*, vol. 65, pp. 1968-1980. Jun. 2018. ISSN 1549-8328 DOI 10.1109/TCSI.2017.2767280
45. P. Maffezzoni, Z. Zhang, **S. Levantino**, L. Daniel, "Variation-aware Modeling of Integrated Capacitors based on Floating Random Walk Extraction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, pp. 2180-2184, Oct. 2018. ISSN 0278-0070 DOI 10.1109/TCAD.2018.2789730

46. M. Mercandelli, L. Grimaldi, L. Bertulessi, C. Samori, A. L. Lacaita, **S. Levantino**, "A Background Calibration Technique to Control the Bandwidth of Digital PLLs," *IEEE Journal of Solid-State Circuits*, vol. 53, Nov. 2018. ISSN 0018-9200 DOI 10.1109/JSSC.2018.2866454
47. D. Cherniak, L. Grimaldi, L. Bertulessi, R, Nonis, C. Samori, **S. Levantino**, "A 23-GHz Low-Phase-Noise Digital Bang-Bang PLL for Fast Triangular and Sawtooth Chirp Modulation," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 3565-3575, Dec. 2018. ISSN 0018-9200. DOI 10.1109/JSSC.2018.2869097
48. A. Garghetti, A. L. Lacaita, **S. Levantino**, "A Novel Single-Inductor Injection-Locked Frequency Divider by Three with Dual-Injection Secondary Locking," *IEEE Trans. on Circuits and Systems-I*, vol. 66, pp. 1737-1745, May 2019. ISSN 1549-8328 DOI 10.1109/TCSI.2018.2871178
49. A. Santiccioli, C. Samori, A. L. Lacaita, **S. Levantino**, "Time-Variant Modeling and Analysis of Multiplying Delay-Locked Loops," *IEEE Trans. on Circuits and Systems-I*, vol. 66, pp. 3775-3785, Jun. 2019. ISSN 1549-8328 DOI 10.1109/TCSI.2019.2918027
50. L. Bertulessi, S. Karman, D. Cherniak, A. Garghetti, C. Samori, A. L. Lacaita**, S. Levantino**, "A 30-GHz Digital Sub-Sampling Fractional-N PLL with -238.6-dB Jitter-Power Figure of Merit in 65-nm LP CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 3493-3502, Sep. 2019. ISSN 0018-9200. DOI 10.1109/JSSC.2019.2940332
51. A. Santiccioli, M. Mercandelli, A. L. Lacaita, C. Samori, **S. Levantino**, "A 1.6-to-3.0-GHz Fractional-N MDLL With a Digital-to-Time Converter Range-Reduction Technique Achieving 397-fs Jitter at 2.5-mW Power," *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 3149-3160, Oct. 2019. ISSN 0018-9200. DOI 10.1109/JSSC.2019.2941259
52. D. Cherniak, M. Mercandelli, L. Bertulessi, F. Padovan, L. Grimaldi, A. Santiccioli, M. Aichner, C. Samori, **S. Levantino**, "A 250-Mb/s direct phase modulator with -42.4-dB EVM based on a 14-GHz digital PLL," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 126-129. 2020. DOI 10.1109/LSSC.2020.3006519
53. L. Avallone, M. P. Kennedy, S. Karman, C. Samori, **S. Levantino**, "Jitter Minimization in Digital PLLs with Mid-Rise TDCs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, pp. 743-752, Mar. 2020. ISSN 1558-0806. DOI 10.1109/TCSI.2019.2959252
54. A. Santiccioli, M. Mercandelli, L. Bertulessi, A. Parisi, D. Cherniak, A.L. Lacaita, C. Samori, **S. Levantino**, "A 66-fs-rms jitter 12.8-to-15.2-GHz fractional-N bang-bang PLL with digital frequency-error recovery for fast locking," *IEEE Journal of Solid-State Circuits*, vol. 55, pp. 3349-3361. Dec. 2020. DOI 10.1109/JSSC.2020.3019344
55. M. Leoncini, **S. Levantino**, M. Ghioni, "Design issues and performance analysis of CCM boost converters with RHP zero mitigation via inductor current sensing," *Journal of Power Electronics*, vol. 21, pp. 285-295, Feb. 2021. DOI 10.1007/s43236-020-00180-x
56. S. Karman, F. Tesolin, **S. Levantino**, C. Samori, "A novel topology of coupled phase-locked loops," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, pp. 989-997, Mar. 2021. DOI 10.1109/TCSI.2020.3043466
57. L. Avallone, M. Mercandelli, A. Santiccioli, M.P. Kennedy, **S. Levantino**, C. Samori, "A comprehensive phase noise analysis of bang-bang digital PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, pp. 2775-2786. Jul. 2021. DOI 10.1109/TCSI.2021.3072344
58. M. Mercandelli, A. Santiccioli, A. Parisi, L. Bertulessi, D. Cherniak, A.L. Lacaita, C. Samori, **S. Levantino**, "A 12.5-GHz fractional-N type-I sampling PLL achieving 58-fs integrated jitter," *IEEE Journal of Solid-State Circuits*, vol. 57, pp. 505-517, Feb. 2022. DOI 10.1109/JSSC.2021.3123827
59. M. Mercandelli, L. Bertulessi, C. Samori, **S. Levantino**, "A digital PLL with multitap LMS-based bandwidth control," *IEEE Solid-State Circuits Letters*, vol. 5, pp. 126-129, 2022. DOI 10.1109/LSSC.2022.3173425
60. L. Bertulessi, D. Cherniak, M. Mercandelli, C. Samori, A.L. Lacaita, **S. Levantino**, "Novel feed-forward technique for digital bang-bang PLL to achieve fast lock and low phase noise," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, pp. 1858-1870, May 2022. DOI 10.1109/TCSI.2022.3146788
61. S.M. Dartizio, F. Tesolin, M. Mercandelli, A. Santiccioli, A. Shehata, S. Karman, **S. Levantino**, "A 12.9-to-15.1-GHz digital PLL based on a bang-bang phase detector with adaptively optimized noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 57, pp. 1723-1735, Jun. 2022. DOI 10.1109/JSSC.2021.3116860
62. A. Garghetti, A.L. Lacaita, D. Seebacher, M. Bassi, **S. Levantino**, "Analysis and design of 8-to-101.6-GHz injection-locked frequency divider by five with concurrent dual-path multi-injection topology," *IEEE Journal of Solid-State Circuits*, vol. 57, pp. 1788-1799, Jun. 2022. DOI 10.1109/JSSC.2021.3134486
63. G. Be, A. Parisi, L. Bertulessi, L. Ricci, L. Scaletti, M. Mercandelli, A.L. Lacaita, **S. Levantino**, C. Samori, A. Bonfanti, "A 900-MS/s SAR-based time-interleaved ADC with a fully programmable interleaving factor and on-chip scalable background calibrations," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 69, pp. 3645-3649, Sep. 2022. DOI 10.1109/TCSII.2022.3182217

64. A. Dago, M. Leoncini, S. Saggini, **S. Levantino**, M. Ghioni, "Hybrid resonant switched-capacitor converter for 48-3.4 V direct conversion," *IEEE Transactions on Power Electronics*, vol. 37, pp. 12998-13002, Nov. 2022. DOI 10.1109/TPEL.2022.3186790
65. S.M. Dartizio, F. Buccoleri, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, D. Cherniak, L. Bertulessi, A. Bevilacqua, C. Samori, A.L. Lacaita, **S. Levantino**, "A fractional-N bang-bang PLL based on type-II gear shifting and adaptive frequency switching achieving 68.6 fs-rms-total-integrated-jitter and 1.56 µs-locking-time," *IEEE Journal of Solid-State Circuits*, vol. 57, pp, 3538-3551, Dec. 2022. DOI 10.1109/JSSC.2022.3206955
66. F. Buccoleri, S.M. Dartizio, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, D. Cherniak, L. Bertulessi, A. Bevilaqua, C. Samori, A.L. Lacaita, **S. Levantino**, "A 72-fs-total-integrated-jitter two-core fractional-N digital PLL with digital period averaging calibration on frequency quadrupler and true-in-phase combiner," *IEEE Journal of Solid-State Circuits*, In Press, pp. 1-13, 2022. DOI 10.1109/JSSC.2022.3228899
67. M. Leoncini, A. Bertolini, P. Melillo, A. Gasparini, **S. Levantino**, M. Ghioni, "Spread-spectrum frequency modulation in a DC/DC converter with time-based control," *IEEE Transactions on Power Electronics*, In press, pp. 1-5. 2022. DOI 10.1109/TPEL.2022.3227954
68. G. Castoro, S.M. Dartizio, A.L. Lacaita, **S. Levantino**, "Phase noise analysis of periodically ON/OFF switched oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, pp. 54-63, Jan. 2023. DOI 10.1109/TCSI.2022.3211177
69. M. Leoncini, A. Dago, A. Bertolini, A. Gasparini, **S. Levantino**, M. Ghioni, "A compact high-efficiency boost converter with time-based control, RHP zero-elimination, and tracking error compensation," *IEEE Transactions on Power Electronics*, pp. 38, pp. 3100-3113, Mar. 2023. DOI 10.1109/TPEL.2022.3222613

IV. Proceedings of International Peer-Reviewed Conferences:

1. C. Samori, A. L. Lacaita, A.Zanchi, **S. Levantino**, F.Torrisi, "Impact of Indirect Stability on Phase Noise Performance of Fully-Integrated LC Tuned VCOs", in *Proceedings of European Solid-State Circuits Conference (ESSCIRC)*, Duisburg (Germany), 21-23 Sept. 1999, pp. 202-205.
2. **S. Levantino**, A.Zanchi, A. Bonfanti, C. Samori, "Fast Simulation Techniques for Noise Analysis of Oscillators", in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS),* Geneva (Switzerland), 28-31 May 2000, vol. II, pp. 156-159. ISBN 0-7803-5482-6. DOI 10.1109/ISCAS.2000.856282
3. A. Zanchi, A. Bonfanti, **S. Levantino**, C. Samori, "General SSCR vs. Cycle-to-Cycle Jitter Relationship with Application to the Phase Noise in PLL", in *Proceedings of IEEE Southwest Symposium on Mixed Signals Design*, Austin (TX, U.S.A.), Feb. 25-27, 2001, pp. 32-37. ISBN 0-7803-6742-1. DOI 10.1109/SSMSD.2001.914933
4. C. Samori, **S. Levantino**, V. Boccuzzi, "A -94dBc/Hz@100kHz, fully-integrated, 5-GHz, CMOS VCO with 18% tuning range for Bluetooth applications", in *Proceedings of IEEE Custom Integrated Circuit Conf. (CICC)*, San Diego (CA, U.S.A.), May 6-9, 2001, pp. 201-204. ISBN 0-7803-6591-7. DOI 10.1109/CICC.2001.929755
5. A. Zanchi, A. Bonfanti, **S. Levantino**, C. Samori, A. L. Lacaita, "Automatic Amplitude Control Loop for a 2-V, 2.5-GHz LC-tank VCO", in *Proceedings of IEEE Custom Integrated Circuit Conf. (CICC),* San Diego (CA, U.S.A.), May 6-9, 2001, pp. 210-213. ISBN 0-7803-6591-7. DOI 10.1109/CICC.2001.929757
6. **S. Levantino**, C. Samori, M. Banu, J. Glas, V. Boccuzzi, "A CMOS IF Sampling Circuit with Reduced Aliasing for Wireless Applications", in *Digest of Technical Papers of the IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco (CA, U.S.A.), Feb. 2002, vol. 2, pp. 328-532. ISBN 0-7803-7335-9. DOI 10.1109/ISSCC.2002.992279
7. **S. Levantino**, C. Samori, M. Banu, J. Glas, V. Boccuzzi, "A CMOS IF Sampling Circuit with Reduced Aliasing for Wireless Applications", in *Digest of Technical Papers of the IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco (CA, U.S.A.), Feb. 2002, vol. 1, pp. 404-405, 477. ISBN 0-7803-7335-9. DOI 10.1109/ISSCC.2002.993103
8. S. Gierkink, **S. Levantino**, R. Frye, V. Boccuzzi, "A Low-Phase-Noise 5GHz Quadrature CMOS VCO Using Common-Mode Inductive Coupling", in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC)*, Florence (Italy), 24-26 Sept. 2002, pp. 539-542.
9. L. Romanò, **S. Levantino**, S. Pellerano, C. Samori, A. Lacaita, "Low Jitter Design of a 0.35-µm-CMOS Frequency Divider Operating up to 3 GHz", in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC),* Florence (Italy), 24-26 Sept. 2002, pp. 611-614.
10. S. Pellerano, C. Samori, **S. Levantino**, A. L. Lacaita, "13.5-mW, 5-GHz WLAN, CMOS Frequency Synthesizer Using a True Single Phase Clock divider", in *Proceedings of the IEEE VLSI Symposium on Circuits,* Kyoto (Japan), 12-14 June 2003, pp. 145-158. ISBN 4-89114-034-8. DOI 10.1109/VLSIC.2003.1221185

11. A. Bonfanti, **S. Levantino**, S. Pellerano, C. Samori, A.L. Lacaita, F. Torrisi, "A Voltage-Controlled Oscillator for IEEE 802.11a and HiperLAN2 Application", in *Proceedings of the European Solid-State Circuits Conference (ESSCIRC),* Estoril (Portugal), 16-18 Sept. 2003, pp. 695-698. ISBN 0-7803-7995-0. DOI 10.1109/ESSCIRC.2003.1257230
12. **S. Levantino**, A. Bonfanti, L. Romanò, C. Samori, A. L. Lacaita, "A 2-GHz Differentially-Tuned VCO with Reduced Flicker Noise Up-Conversion", in *Proceedings of 21st Norchip Conference,* Riga (Latvia), 10-11 Nov. 2003, pp. 163-166.
13. S. Pellerano, **S. Levantino**, C. Samori, A. L. Lacaita, "A 2-GHz Low-Power Low-Noise CMOS 32/33 Prescaler", in *Proceedings of 21st Norchip Conference,* Riga (Latvia), 10-11 Nov. 2003, pp. 256-259.
14. A. Bonfanti, **S. Levantino**, L. Romanò, C. Samori, A. Lacaita, "A Varactor Configuration Minimizing Flicker Noise Up-Conversion in VCOs", in *Proceedings of the IEEE Workshop on Wireless Circuits and Systems (WoWCAS)* 2004, 21-22 May 2004, Vancouver (Canada), pp. 25-26.
15. L. Romanò, **S. Levantino**, A. Bonfanti, C. Samori, A. Lacaita, "Phase Noise and Accuracy in Quadrature Oscillators" in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)* 2004, Vancouver (Canada), vol. I, pp. 161-164, 23-26 May 2004. ISBN 0-7803-8251-X. DOI 10.1109/ISCAS.2004.1328156
16. **S. Levantino**, L. Romanò, C. Samori, A. Lacaita, "Fast-Switching Analog PLL with Finite-Impulse Response" in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)* 2004, vol. IV, pp. 165-168, 23-26 May 2004, Vancouver, Canada. ISBN 0-7803-8251-X. DOI 10.1109/ISCAS.2004.1328966
17. **S. Levantino**, X. Wang, P. Andreani, C. Samori, A. Lacaita, "A Circuit Technique Improving the Image Rejection of RF Front-Ends" in *Digest of Technical Papers of the IEEE 2004 Symposia on VLSI Technology and Circuits,* 17-19 June 2004, Honolulu, (HI, U.S.A.), pp. 368-371. ISBN 0-7803-8287-0. DOI 10.1109/VLSIC.2004.1346618
18. L. Romanò, C. Samori, **S. Levantino**, A. Bonfanti, A. L. Lacaita, "A Multi-tank LC-oscillator," in *Proceedings of the 11th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* Tel Aviv (Israel), 13-15 Dec. 2004, pp. 29-32. ISBN 0-7803-8715-5. DOI 10.1109/ICECS.2004.1399606
19. **S. Levantino**, A. Bonfanti, L. Romanò, C. Samori, A. L. Lacaita, "Differential tuning oscillator with reduced flicker noise upconversion," in *Proceedings of the 11-th IEEE International Conference on Electronics, Circuits and Systems (ICECS),* Tel Aviv (Israel), 13-15 Dec. 2004, pp. 33-36. ISBN 0-7803-8715-5. DOI 10.1109/ICECS.2004.1399607
20. S. Pellerano, **S. Levantino**, C. Samori, A.L. Lacaita, "A Dual-band Frequency Synthesizer for 802.11a/b/g with Fractional-spur Averaging Technique," in *Digest of Technical Papers of the IEEE Int. Solid-State Circuits Conference (ISSCC),* San Francisco (CA, U.S.A.), 6-10 Feb. 2005, vol. 1, pp. 104-105, 587. ISSN 0193-6530. ISBN 0-7803-8904-2. DOI 10.1109/ISSCC.2005.1493890
21. L. Panseri, L. Romanò, **S. Levantino**, C. Samori, A. Lacaita, "Low-power CMOS IEEE 802.11a/g signal separator for outphasing transmitter," in *Proceedings of the IEEE 2006 Custom Integrated Circuits Conference (CICC),* 10-13 Sept. 2006, San Jose (CA, U.S.A.), pp. 133-136. ISBN 1-4244-0075-9. DOI 10.1109/CICC.2006.320850
22. L. Panseri, L. Romanò, **S. Levantino**, C. Samori, A. Lacaita, "Low-Power All-Analog Component Separator for an 802.11a/g LINC Transmitter", in *Proceedings of the 32nd European Solid-State Circuits Conference (ESSCIRC)* 2006, Montreaux (Switzerland), 19-21 Sept. 2006, pp. 271-274. ISSN 1930-8833. ISBN 1-4244-0303-0. DOI 10.1109/ESSCIR.2006.307583
23. M. Zanuso, **S. Levantino**, D. Tasca, D. Raiteri, C. Samori, A. L. Lacaita, "A Glitch-Corrector Circuit for Low-Spur ADPLLs," in *Proceedings of IEEE International Conference on Electronics, Circuits and Systems 2009 (ICECS),* Medina (Tunisia), 13-16 Dec. 2009, pp. 595-598. ISBN 978-1-4244-5090-9. DOI 10.1109/ICECS.2009.5410853
24. **S. Levantino**, M. Zanuso, D. Tasca, C. Samori, A. L. Lacaita, "An All-Digital Architecture for Low-Jitter Regulated Delay Lines", in *Proceedings of IEEE International Conference on Electronics, Circuits and Systems 2009 (ICECS),* Medina (Tunisia), 13-16 Dec. 2009, pp. 603-606. ISBN 978-1-4244-5090-9. DOI 10.1109/ICECS.2009.5410855
25. **S. Levantino**, M. Zanuso, C. Samori, A. L. Lacaita, "Suppression of flicker noise upconversion in a 65nm CMOS VCO in the 3.0-to-3.6GHz band," in *Digest of Technical Papers of the 2010 IEEE International Solid-State Circuits Conference (ISSCC),* San Francisco (California), 7-11 Feb. 2010, pp. 50-51. ISSN 0193-6530. ISBN 978-1-4244-6033-5. DOI 10.1109/ISSCC.2010.5434054
26. M. Zanuso, **S. Levantino**, C. Samori, A. L. Lacaita, "A 3MHz-BW 3.6GHz digital fractional-N PLL with sub-gate-delay TDC, phase-interpolation divider, and digital mismatch cancellation," in *Digest of Technical Papers of the IEEE Int. Solid-State Circuits Conference (ISSCC),* San Francisco (California), 7-11 Feb. 2010, pp. 476-477. ISSN 0193-6530. ISBN 978-1-4244-6033-5. DOI 10.1109/ISSCC.2010.5433842

27. D. Tasca, M. Zanuso, **S. Levantino**, C. Samori, "An automatic retiming system for asynchronous fractional frequency dividers," in *Proceedings of 2010 Conference on Ph.D. Research in Microelectronics and Electronics (PRIME),* Berlin (Germany), 18-21 Jul. 2010, pp. 1-4. ISBN 978-1-4244-7905-4. ISBN 978-1-4244-7905-4.
28. G. Marzin, L. Collamati, **S. Levantino**, C. Samori, "Folding of Phase Spectrum in Phase-Locked Loops," in *Proceedings of 13th Edition of IEEJ International Analog VLSI Workshop (AVLSIWS),* Pavia (Italy), 8-10 Sept. 2010.
29. M. Zanuso, **S. Levantino**, A. Puggelli, C. Samori, A. L. Lacaita, "Time-to-digital converter with 3-ps resolution and digital linearization algorithm," in *Proceedings of the 2010 IEEE European Solid-State Circuits Conference (ESSCIRC),* Seville (Spain), 14-16 Sept. 2010, pp. 262-265. ISSN 1930-8833. ISBN 978-1-4244-6662-7. DOI 10.1109/ESSCIRC.2010.5619879
30. D. Tasca, M. Zanuso, G. Marzin, **S. Levantino**, C. Samori, A. L. Lacaita, "A 2.9-to-4.0GHz fractional-N digital PLL with Bang-Bang phase detector and 560fsrms integrated jitter at 4.5mw power," in *Digest of Technical Papers of the IEEE Int. Solid-State Circuits Conference (ISSCC),* San Francisco (California), 20-24 Feb. 2011, pp. 88-89. ISSN 0193-6530. ISBN 978-1-61284-303-2. DOI 10.1109/ISSCC.2011.5746231
31. C. Samori, M. Zanuso, **S. Levantino**, A. L. Lacaita, "Multipath Adaptive Cancellation of Divider Non-Linearity in Fractional-N PLLs", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)* 2011, Rio de Janeiro (Brazil), 15-18 May 2011, pp. 418-421. ISSN 0271-4302- ISBN 978-1-4244-9473-6. DOI 10.1109/ISCAS.2011.5937591
32. P. Maffezzoni, **S. Levantino**, C. Samori, A. Lacaita, D. D'Amore, M. Santomauro, "Behavioral Phase-Noise Analysis of Charge-Pump Phase-Locked Loops," in Pr*oceedings of IEEE European Conference on Circuit Theory and Design (ECCTD),* Linkoping (Sweden), 29-31 Aug. 2011, pp. 357-360. ISBN 978-1-4577-0617-2. DOI 10.1109/ECCTD.2011.6043360
33. G. Marzin, **S. Levantino**, C. Samori, A. L. Lacaita, "20Mb/s Phase Modulator Based on a 3.6GHz Digital PLL with -36dB EVM at 5mW Power," in *Digest of Technical Papers of the IEEE Int. Solid-State Circuits Conference (ISSCC),* San Francisco (California), 19-23 Feb. 2012, pp. 342-344. ISSN 0193-6530. ISBN 978-146730373-6. DOI 10.1109/ISSCC.2012.6177007
34. **S. Levantino**, D. Tasca, G. Marzin, M. Zanuso, C. Samori, A. Lacaita, "A Wideband Fractional-N PLL with Suppressed Charge-Pump Noise and Automatic Loop Filter Calibration," in *Digest of 2012 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* Montreal (Canada), 17-19 Jun. 2012, pp. 177-180. ISSN 1529-2517. ISBN 978-1-4673-0413-9. DOI 10.1109/RFIC.2012.6242258
35. F. Pepe, A. Bonfanti, **S. Levantino**, P. Maffezzoni, C. Samori, A. L. Lacaita, "An efficient linear-time variant simulation technique of oscillator phase sensitivity function," in *Proceedings of 2012 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD),* Seville (Spain), Sept. 2012, pp. 17-20. ISBN 978-146730686-7. DOI 10.1109/SMACD.2012.6339406
36. G. Marzin, A. Fenaroli, G. Marucci, **S. Levantino,** C. Samori, A.L. Lacaita, "A spur cancellation technique for MDLL-based frequency synthesizers," in *Proceedings of 2013 IEEE International Symposium on Circuits and Systems (ISCAS),* Beijing (China), 19-23 May 2013, pp. 165-168. ISSN 0271-4302. ISBN 978-1-4673-5760-9. DOI 10.1109/ISCAS.2013.6571808
37. G. Marucci, **S. Levantino**, P. Maffezzoni, C. Samori, "Minimum-jitter design of bang-bang PLLs in the presence of $1/f^2$ and $1/f^3$ DCO noise," in *Proceedings of 2013 IEEE International Symposium on Circuits and Systems (ISCAS),* Beijing (China), 19-23 May 2013, pp. 173-176. ISSN 0271-4302. ISBN 978-1-4673-5760-9. DOI 10.1109/ISCAS.2013.6571810
38. A. Fenaroli, **S. Levantino**, C. Samori, A.L. Lacaita, "Background adaptive linearization of high-speed digital-to-analog Converters Proceedings," in *Proceedings of 2013 IEEE International Symposium on Circuits and Systems (ISCAS),* Beijing (China), 19-23 May 2013, pp. 582-585. ISSN 0271-4302. ISBN 978-1-4673-5760-9. DOI 10.1109/ISCAS.2013.6571909
39. G. Marucci, **S. Levantino**, P. Maffezzoni, C. Samori, "An efficient method to compute phase-noise in injection-locked frequency dividers," in *Proceedings of 2013 IEEE International Symposium on Circuits and Systems (ISCAS),* Beijing (China), 19-23 May 2013, pp. 1753-1756. ISSN 0271-4302. ISBN 978-1-4673-5760-9. DOI 10.1109/ISCAS.2013.6572204
40. F. Pepe, A. Bonfanti, **S. Levantino,** P. Maffezzoni C. Samori, A.L. Lacaita, "Simulating phase noise induced from cyclostationary noise sources," in *Proceedings of 2013 IEEE International Symposium on Circuits and Systems (ISCAS),* Beijing (China), 19-23 May 2013, pp. 2686-2689. ISSN 0271-4302. ISBN 978-1-4673-5760-9. DOI 10.1109/ISCAS.2013.6572432
41. F. Pepe, A. Bonfanti, **S. Levantino,** C. Samori, A.L. Lacaita, "Reducing flicker noise up-conversion in a 65-nm CMOS VCO in the 1.6-to-2.6 GHz band," in *Proceedings of SPIE Conference on VLSI Circuits and Systems,* Grenoble (France), 24-26 Apr. 2013. ISSN 0277786X. ISBN 978-081949561-7. DOI 10.1117/12.2016841

42. F. Pepe, A. Bonfanti, **S. Levantino,** P. Maffezzoni, C. Samori, A.L. Lacaita, "A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators," in *Proceedings of SPIE Conference on VLSI Circuits and Systems*, Grenoble (France), 24-26 Apr. 2013. ISSN 0277786X. ISBN 978-081949561-7. DOI 10.1117/12.2016873
43. F. Pepe, A. Bonfanti, **S. Levantino,** C. Samori, A.L. Lacaita, "A wideband voltage-biased LC oscillator with reduced flicker noise up-conversion," in *Digest of 2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* Seattle (Washington), 2-4 Jun. 2013, pp. 27-30. ISSN 1529-2517. ISBN 978-1-4673-6059-3. DOI 10.1109/RFIC.2013.6569513
44. **S. Levantino** and C. Samori, "Nonlinearity cancellation in digital PLLs **(Invited paper)**," in *Proceedings of the 2013 Custom Integrated Circuits Conference*, San Jose (California), 22-25 Sept. 2013, pp. 1-8. ISSN 08865930. ISBN 978-146736146-0. DOI 10.1109/CICC.2013.6658472
45. **S. Levantino**, "Advanced digital phase-locked loops," in *Proceedings of the 2013 Custom Integrated Circuits Conference*, San Jose (California), 22-25 Sept. 2013, pp. 1-95. ISSN 08865930. ISBN 978-146736146-0. DOI 10.1109/CICC.2013.6658505
46. G. Marucci, A. Fenaroli, G. Marzin, **S. Levantino**, C. Samori, A.L. Lacaita, "A 1.7GHz MDLL-Based Fractional-N Frequency Synthesizer with 1.4ps RMS Integrated Jitter and 3mW Power Using a 1b TDC," in *Digest of Technical Papers of the IEEE Int. Solid-State Circuits Conference (ISSCC),* San Francisco (California), 9-13 Feb. 2014, pp. 360-361. ISSN 0193-6530. ISBN 978-1-4799-0918-6. DOI 10.1109/ISSCC.2014.6757469
47. G. Marzin, **S. Levantino**, C. Samori, A.L. Lacaita, "A Background Calibration Technique to Control Bandwidth in Digital PLLs," in *Digest of Technical Papers of the IEEE Int. Solid-State Circuits Conference (ISSCC)*, San Francisco (California), 9-13 Feb. 2014, pp. 54-55. ISSN 0193-6530. ISBN 978-1-4799-0918-6. DOI 10.1109/ISSCC.2014.6757335
48. F. Pepe, A. Bonfanti, **S. Levantino,** A. L. Lacaita, "Impact of Non-Quasi-Static Effects on $1/f^3$ Phase Noise in a 1.9-to-2.6-GHz Oscillator," in *Digest of 2014 IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* Tampa (Florida), 1-3 Jun. 2014, pp. 425-428. ISSN 1529-2517. ISBN 978-1-4799-3862-9. DOI 10.1109/RFIC.2014.6851758
49. **S. Levantino**, "Bang-Bang Digital PLLs," **(Invited Paper)** in *Proceedings of the 2016 IEEE European Solid-State Circuits Conference (ESSCIRC),* Lausanne (Switzerland), 12-15 Sept. 2016, pp. 329-332. ISSN 1930-8833. ISBN 978-1-5090-2972-3. DOI 10.1109/ESSCIRC.2016.7598309
50. T.M. Vo, **S. Levantino**, C. Samori, "Analysis of Fractional-N Bang-Bang Digital PLLs using Phase Switching Technique," in *Proceedings of 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Lisbon (Portugal), 27-30 June 2016, pp. 1-4. ISBN 978-1-5090-0493-5. DOI 10.1109/PRIME.2016.7519545
51. **S. Levantino**, L. Grimaldi, C. Samori, "Analysis of Adaptive Pre-Distortion in DTC-based Digital Fractional-N PLLs," in *Proceedings of 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Lisbon (Portugal), 27-30 June 2016, pp. 1-4. ISBN 978-1-5090-0493-5. DOI 10.1109/PRIME.2016.7519527
52. L. Bertulessi, **S. Levantino**, C. Samori, "Analysis of Power Efficiency in High-Performance Class-B Oscillators," in *Proceedings of 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Lisbon (Portugal), 27-30 June 2016, pp. 1-4. ISBN 978-1-5090-0493-5. DOI 10.1109/PRIME.2016.7519525
53. D. Cherniak, **S. Levantino**, C. Samori, "Wideband Chirp Generation techniques in Digital Phase-Locked Loops," in *Proceedings of 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Lisbon (Portugal), 27-30 June 2016, pp. 1-4. ISBN 978-1-5090-0493-5. DOI 10.1109/PRIME.2016.7519479
54. T. M. Vo, C. Samori, A. L. Lacaita, **S. Levantino**, "A novel segmentation scheme for DTC-based ΔΣ fractional-N PLL," in *Proceedings of International Circuits and Systems Conf. (ISCAS),* Baltimore (MD, USA), 28-31 May 2017, pp 1-4. ISBN 978-1-4673-6853-7 DOI 10.1109/ISCAS.2017.8050285
55. D. Cherniak, **S. Levantino**, C. Samori, R. Nonis, "Analysis of millimeter-wave digital frequency modulators for ubiquitous sensors and radars," in *Proceedings of International Circuits and Systems Conf. (ISCAS),* Baltimore (MD, USA), 28-31 May 2017, pp 1-4. ISBN 978-1-4673-6853-7 DOI 10.1109/ISCAS.2017.8050549
56. D. Cherniak, L. Grimaldi, L. Bertulessi, C. Samori, R. Nonis, **S. Levantino**, "A 23GHz Low-Phase-Noise Digital Bang-Bang PLL for Triangular and Saw-tooth Chirp Modulation," in *Digest of 2018 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 11-15 Feb. 2018, pp. 248-249. ISBN 978-1-5090-4940-0 DOI 10.1109/ISSCC.2018.8310277
57. L. Bertulessi, L. Grimaldi, D. Cherniak, C. Samori, **S. Levantino**, "A Low-Phase-Noise Digital Bang-Bang PLL with Fast Lock Over a Wide Lock Range," in *Digest of 2018 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 11-15 Feb. 2018, pp. 252-253. ISBN 978-1-5090-4940-0 DOI 10.1109/ISSCC.2018.8310279
58. A. Garghetti, A. L. Lacaita, **S. Levantino**, "A Low-Power and Wide-Locking-Range Injection-Locked Frequency Divider by Three with Dual-Injection Divide-by-Two Technique," in *Proceedings of International Circuits and*

Systems Conf. (ISCAS), Florence (Italy), 27-30 May 2018, pp 1-4. ISBN 978-1-5386-4881-0 DOI 10.1109/ISCAS.2018.8350910

59. A. Truppi, C. Samori, A. L. Lacaita, **S. Levantino**, M. Ronchi, M. Sosio, "Impact of CMOS Scaling on Switched-Capacitor Power Amplifiers," in *Proceedings of International Circuits and Systems Conf. (ISCAS),* Florence (Italy), 27-30 May 2018, pp 1-4. ISBN 978-1-5386-4881-0 DOI 10.1109/ISCAS.2018.8351752
60. D. Cherniak, L. Grimaldi, C. Samori, **S. Levantino**, "Adaptive Digital Pre-Emphasis for PLL-Based FMCW Modulators," in *Proceedings of International Circuits and Systems Conf. (ISCAS),* Florence (Italy), 27-30 May 2018, pp 1-4. ISBN 978-1-5386-4881-0 DOI 10.1109/ISCAS.2018.8351846
61. T. M. Vo, C. Samori, **S. Levantino**, "A Novel LMS-Based Calibration Scheme for Fractional-N Digital PLLs," in *Proceedings of International Circuits and Systems Conf. (ISCAS),* Florence (Italy), 27-30 May 2018, pp 1-4. ISBN 978-1-5386-4881-0 DOI 10.1109/ISCAS.2018.8351321
62. **S. Levantino**, "Digital phase-locked loops," *2018 IEEE Custom Integrated Circuits Conference (CICC),* San Diego (CA, USA), 8-11 April 2018. ISBN 978-1-5386-2483-8 DOI 10.1109/CICC.2018.8357109
63. D. Cherniak, L. Grimaldi, M. Bassi, C. Samori, **S. Levantino**, "A 15.6-18.2 GHz Digital Bang-Bang PLL with -63dBc In-Band Fractional Spur," in Proc. of 2018 IEEE Radio Frequency Integrated Circuits Conference (RFIC), Philadelphia (PA, USA), 10-12 Jun. 2018. ISBN 978-1-5386-4545-1 DOI 10.1109/RFIC.2018.8428846
64. **S. Levantino**, C. Samori, "Digitally-Assisted Frequency Synthesizers for Fast Chirp Generation in mm-Wave radars," in *Proc. of 2018 19th International Radar Symposium (IRS)*, Bonn (Germany), 20-22 Jun. 2018. ISBN 978-3-7369-9545-1 DOI 10.23919/IRS.2018.8447994
65. A. Garghetti, A. L. Lacaita, **S. Levantino,** "A Single-Inductor Two-Step-Mixing Injection-Locked Frequency Divider by Four with Concurrent Tail-Injection," *2018 25th IEEE International Conference on Electronics Circuits and Systems (ICECS)*, Bordeaux, France, 9-12 Dec. 2018. ISBN 978-1-5386-9562-3 DOI 10.1109/ICECS.2018.8618045
66. L. Grimaldi, L. Bertulessi, S. Karman, D. Cherniak, A. Garghetti, C. Samori, A. L. Lacaita, **S. Levantino**, "A 30GHz Digital Sub-Sampling Fractional-N PLL with 198fs rms Jitter in 65nm LP CMOS," in *Digest of 2019 International Solid-State Circuits (ISSCC)*. San Francisco (CA, USA). 17-21 Feb. 2019. ISBN 978-1-5386-8531-0 DOI 10.1109/ISSCC.2019.8662411
67. D. Cherniak, C. Samori, **S. Levantino**, "Digitally-Intensive Fast Frequency Modulators for FMCW Radars in CMOS (**Invited Paper**)," in *Digest of 2019 IEEE Custom Integrated Circuits Conference (CICC),* Austin (TX, USA), 14-17 April 2019.
68. A. Santiccioli, M. Mercandelli, A.L. Lacaita, C. Samori, **S. Levantino**, "A 1.6-to-3.0-GHz Fractional-N MDLL with a Digital-to-Time Converter Range-Reduction Technique Achieving 397fs Jitter at 2.5-mW Power," in *Digest of 2019 IEEE Custom Integrated Circuits Conference (CICC),* Austin (TX, USA), 14-17 April 2019.
69. A. Santiccioli, M. Mercandelli, L. Bertulessi, A. Parisi, D. Cherniak, A. L. Lacaita, C. Samori, **S. Levantino**, "17.2 A 66fsrmsJitter 12.8-to-15.2GHz Fractional-N Bang-Bang PLL with Digital Frequency-Error Recovery for Fast Locking," in *Digest of 2020 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 11-15 Feb. 2020, pp. 252-253. ISBN 978-1-7281-3205-1 DOI 10.1109/ISSCC19947.2020.9063094
70. M. Mercandelli, A. Santiccioli, A. Parisi, L. Bertulessi, D. Cherniak, A. L. Lacaita, C. Samori, **S. Levantino**, "17.5 A 12.5GHz Fractional-N Type-I Sampling PLL Achieving 58fs Integrated Jitter," in *Digest of 2020 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 11-15 Feb. 2020, pp. 252-253. ISBN 978-1-7281-3205-1 DOI 10.1109/ISSCC19947.2020.9063135
71. T. Rosa, M. Leoncini, **S. Levantino**, M. Ghioni, "A novel start-up technique for time-based boost converters with seamless PFM/PWM transition," in Proc. of *IEEE International Symposium on Circuits and Systems (ISCAS)*, October 2020.
72. M. Mercandelli, A. Santiccioli, S.M. Dartizio, A. Shehata, F. Tesolin, K. Saleh, L. Bertulessi, F. Buccoleri, L. Avallone, A. Parisi, D. Cherniak, A. L. Lacaita, M.P. Kennedy, C. Samori, **S. Levantino**, "A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter," in *Digest of 2021 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 13 Feb. 2021, pp. 445-447. ISBN 978-172819549-0 DOI 10.1109/ISSCC42613.2021.9365768
73. M. Mercandelli, A. Santiccioli, S.M. Dartizio, F. Tesolin, K. Saleh, A. Shehata, L. Bertulessi, F. Buccoleri, L. Avallone, A. Parisi, A. L. Lacaita, M.P. Kennedy, C. Samori, **S. Levantino**, "32.8 A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays," in *Digest of 2021 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 13 Feb. 2021, pp. 456-458. ISBN 978-172819549-0 DOI 10.1109/ISSCC42613.2021.9365972
74. A. Garghetti, A.L. Lacaita, D. Seebacher, M. Bassi, **S. Levantino**, "A 13.6-69.1GHz 5.6mW Ring-Type Injection-Locked Frequency Divider by Five with 20% Continuous Locking Range and Operation up to 101.6GHz in 28nm

CMOS," in *Proc. of the Custom Integrated Circuits Conference (CICC)*, Apr. 2021. DOI 10.1109/CICC51472.2021.9431565

75. M. Mercandelli, L. Bertulessi, C. Samori**, S**. **Levantino**, "A 3.7-To-4.1GHz Narrowband Digital Bang-Bang PLL with a Multitaps LMS Algorithm to Automatically Control the Bandwidth Achieving 183fs Integrated Jitter," in *Proc. of IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2021. DOI 10.1109/A-SSCC53895.2021.9634706
76. S. Karman, F. Tesolin, A. Dago, M. Mercandelli, C: Samori, **S. Levantino**, "A 18.9-22.3GHz Dual-Core Digital PLL with On-Chip Power Combination for Phase Noise and Power Scalability," in *Digest of Papers of IEEE Radio Frequency Integrated Circuits Symposium* (RFIC), Jun. 2021, pp. 67-70. DOI 10.1109/RFIC51843.2021.9490476
77. M. Leoncini, A. Bertolini, A. Gasparini, **S. Levantino**, M. Ghioni, "An 800-mA Time-Based Boost Converter in 0.18m BCD with Right-Half-Plane Zero Elimination and 96% Power Efficiency," in *Proc. of IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, Sep. 2021, pp. 223-226, DOI 10.1109/ESSCIRC53450.2021.9567838
78. G. Amendola, L. Boccia, F. Centurelli, P. Chevalier, A. Fonte, S. Karman, **S. Levantino**, A. Mazzanti, C. Mustacchio, A. Pallotta, I. Petricli, C. Samori, F. Tesolin, P. Tommasino, A. Traversa, A. Trifiletti, "SiGe BiCMOS Building Blocks for E- and D-Band Backhauling Front-Ends," in *Proc. of 16th European Microwave Integrated Circuits Conference (EuMIC)*, Sep. 2021. DOI 10.23919/EuMIC50153.2022.9783703
79. S.M. Dartizio, F. Buccoleri, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, D. Cherniak, L. Bertulessi, A. Bevilacqua, C. Samori, A.L. Lacaita, **S. Levantino**, "A 68.6fs_rms-Total-integrated-Jitter and 1.5us-Locking-Time Fractional-N Bang-Bang PLL Based on Type-II Gear Shifting and Adaptive Frequency Switching," in *Digest of 2022 International Solid-State Circuits (ISSCC)*, San Francisco (CA, USA), 20-26 Feb. 2022, pp. 386-388. ISBN 978-172819549-0 DOI 10.1109/ISSCC42614.2022.9731683
80. **S. Levantino**, "Recent Advances in High-Performance Frequency Synthesizer Design," (**Invited Paper**) in *Proc. of the Custom Integrated Circuits Conference*, Apr. 2022. DOI 10.1109/CICC53496.2022.9772842
81. F. Buccoleri, S.M. Dartizio, F. Tesolin, L. Avallone, A. Santiccioli, A. Iesurum, G. Steffan, A. Bevilacqua, L. Bertulessi, D. Cherniak, C. Samori, A.L. Lacaita, **S. Levantino**, "A 9GHz 72fs-Total-Integrated-Jitter Fractional-N Digital PLL with Calibrated Frequency Quadrupler," in *Proc. of the Custom Integrated Circuits Conference*, Apr. 2022. DOI 10.1109/CICC53496.2022.9772796
82. A. Dago, M. Leoncini, A. Cattani, **S. Levantino**, M. Ghioni, "A Novel Common-Gate Comparator with Auto-Zeroing Offset Cancellation," in *Proc. of 17th International Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2022, pp. 81-84. DOI 10.1109/PRIME55000.2022.9816755
83. M. Leoncini, P. Melillo, A. Bertolini, **S. Levantino**, M. Ghioni, "Integrated Loop-Gain Measurement Circuit for DC/DC Boost Converters with Time-Based Control," in *Proc. of 17th International Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2022, pp. 253-256. DOI 10.1109/PRIME55000.2022.9816761
84. P. Melillo, A. Dago, A. Gasparini, **S. Levantino**, M. Ghioni, "A Novel Feedforward Technique for Improved Line Transient in Time-Based-Controlled Boost Converters," in *Proc. of 17th International Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2022, pp. 257-260. DOI 10.1109/PRIME55000.2022.9816834
85. L. Scaletti, G. Bè, A. Parisi, L. Bertulessi, L. Ricci, M. Mercandelli, **S. Levantino**, C. Samori, A. Bonfanti, "A 10.2-ENOB, 150-MS/s Redundant SAR ADC With a Quasi-Monotonic Switching Algorithm for Time-Interleaved Converters," in *Proceedings of 20th IEEE International Interregional NEWCAS Conference*, NEWCAS 2022, pp. 20-24. DOI 10.1109/NEWCAS52662.2022.9842195
86. L. Ricci, L. Scaletti, G. Be, L. Bertulessi, **S. Levantino**, C. Samori, A. Bonfanti, "Concurrent Effect of Redundancy and Switching Algorithms in SAR ADCs," in *Proc. of 2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2022, pp. 900-904. DOI 10.1109/ISCAS48785.2022.9937809
87. **S. Levantino**, "Frequency Synthesizers for 5G Applications," (**Invited Paper**) *in Proc. of IEEE/IFIP International Conference on VLSI and System-on-Chip, VLSI-SoC*, Oct. 2022. DOI 10.1109/VLSI-SoC54400.2022.9939577

V. Editorials:

1. **S. Levantino**, "Introduction to the Special Section on the 2015 Radio Frequency Integrated Circuits Symposium," *IEEE Journal of Solid-State Circuits*, vol. 51, pp. 1064-1065, May 2016. ISSN 0018-9200. DOI 10.1109/JSSC.2016.2549478
2. R.T. Yazicigil, **S. Levantino**, "Special Section on the 47th IEEE European Solid-State Circuits Conference (ESSCIRC)," *IEEE Journal of Solid-State Circuits*, 57 (7), pp. 1955-1956. DOI 10.1109/JSSC.2022.3174500

3. A. Bevilacqua, **S. Levantino**, H. Wang, H. "Session 20 overview: High-performance VCOs rf subcommittee," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 64, pp. 292-293. DOI 10.1109/ISSCC42613.2021.9365970

VI. Patents:

1. S. Gierkink, **S. Levantino**, *"Phase-error suppressor and a method of suppressing phase-error,"* US Patent App. 10/628,162, July 2004. US2004127172A1 (http://www.google.com/patents/US20040127172)
2. S. Gierkink, V. Boccuzzi, R.C. Frye, **S. Levantino**, "*Quadrature voltage controlled oscillator utilizing common-mode inductive coupling,"* US Patent (**issued**), no. 6,911,870. 28 Jun. 2005. (http://www.google.com/patents/US6911870).
3. **S. Levantino**, M. Zanuso, C. Samori, "*Oscillatore elettronico con ridotto rumore di fase"*, Domanda di brevetto italiano ITMI2009A000125, Feb. 2009. (https://patents.google.com/patent/ITMI20090125A1)
4. **S. Levantino**, M. Zanuso, C. Samori, *"A time-digital converter and an electronic system implementing the converter*", International Patent Application, PCT/EP2010/050440, Jan. 2010. (http://www.google.com/patents/WO2010084083A1)
5. M. Zanuso, **S. Levantino**, C. Samori, *"Electronic device for generating a fractional frequency*", US Patent (**issued**), no. 8,571,161. 29 Oct. 2013 (http://www.google.com/patents/US8571161)
6. D. Cherniak**, S. Levantino**, M. Tiebout, R. Nonis, "*Digital frequency synthesizer with robust injection locked divider*", US Patent (**issued**), US15/438,438, 23 Aug. 2018 (https://patents.google.com/patent/US11233520B2)
7. D. Cherniak, S. **Levantino**, M. Mercandelli, "*Radar signal modulator with bandwidth compensation and frequency offset sequence*", US Patent (**issued**), US11454715B2, Dec. 2019 (https://patents.google.com/patent/US20210173070A1)
8. D. Cherniak, S. **Levantino**, A. Santiccioli, "*Phase locked loop with parallel phase detection circuit*", US Patent US11418199B1, May 2021 (https://patents.google.com/patent/DE102022112222A1)
9. A. Gasparini, A. Bertolini, M. Leoncini, M. Ghioni, S. **Levantino**, "*DC-DC converter apparatus with time-based control loop and corresponding control method, and computer program product*", US Patent, US2022216789A1, Jan. 2021 (https://patents.google.com/patent/US20220216789A1)
10. A. Dago, A. Gasparini, O.E. Zambetti, S. **Levantino**, M. Ghioni, "*Switched capacitor converter, corresponding method, power supply system and electronic device*", US Patent, US2023034786A1, July 2021.